WIDEBAND PHASE-LOCKED LOOPS WITH HIGH SPECTRAL PURITY FOR WIRELESS COMMUNICATIONS

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Kun Seok Lee

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WIDEBAND PHASE-LOCKED LOOPS WITH HIGH SPECTRAL PURITY FOR WIRELESS COMMUNICATIONS

Approved by:

Dr. J. Stevenson Kenney, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Erik I. Verriest
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Chang-Ho Lee
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Yunho Lee

Samsung RFIC Design Center

Dr. Kevin T. Kornegay
School of Electrical and Computer Engineering
Georgia Institute of Technology

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"Have I not commanded you? Be strong and courageous. Do not be afraid; do not be discouraged, for the LORD your God will be with you wherever you go."

Joshua 1:9

First of all, I would like to thank God for having made everything possible by giving me strength and wisdom in my life.

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LIST OF SYMBOLS AND ABBREVIATIONS

ADPLL	*All Digital PLL*
AFC	*Adaptive Frequency Calibration*
BPSK	*Binary Phase Shift Keying*
CDMA	*Code Division Multiple Access*
CMOS	*Metal-Oxide-Semiconductor*
CORDIC	*COordinate Rotation DIgital Computer*
CP	*Charge-Pump*
CPU	*Central Processing Unit*
DAC	*Digital-to-Analog Convertor*
DCO	*Digitally Controlled Oscillator*
DCXO	*Digitally Controlled Crystal Oscillator*
DSM	*Delta-Sigma Modulator*
EDGE	*Enhanced data rates for GSM evolution*
EVM	*Error Vector Magnitude*
FN-PLL	*Fractional-N PLL*
FS	*Frequency Synthesizer*
GSM	*Global Systems for Mobile communications*
GPS	*Global Positioning* System
GUI	*Graphical User Interface*
HDL	*Hardware Description Language*
HSPA	*High Speed Packet Access*

IN-PLL	*Integer-N PLL*
I/Q	*Inphase and Quadrature*
LCD	*Liquid Crystal Display*
LO	*Local Oscillator*
LPF	*Low Pass Filter*
LSB	*Least Significant Bit*
LTE	*Long- Term Evolution*
MASH	*Multi-Stage Noise Shaping*
MIM	*Metal-Insulator-Metal*
MP3	*Moving Picture experts group layer-3*
OFDM	*Orthogonal Frequency Division Multiplexing*
PA	*Power Amplifier*
PAPR	*Peak-to-Average-Power Ratio*
PFD	*Phase Frequency Detector*
PLL	*Phase-Locked Loop*
Q-factor	*Quality-factor*
QAM	*Quadrature Amplitude Modulation*
QPSK	*Quadrature Phase Shift Keying*
Rx	*Reception*
RF	*Radio Frequency*
RMS	*Root Mean Square*
SAW	*Surface Acoustic Wave*
SNR	*Signal to Noise Ratio*

SOI	*Silicon On Insulator*
SPI	*Serial Peripheral Interface*
SSB	*Single-Side Band*
STI	*Shallow Trench Isolation*
Tx	*Transmission*
TDMA	*Time Division Multiple Access*
USB	*Universal Serial Bus*
VCO	*Voltage-Controlled Oscillator*
VC-TCXO	*Voltage Controlled- Temperature Compensated Oscillator*
WCDMA	*Wideband CDMA*
WLAN	*Wireless Local Area Network*
WiMax	*Worldwide interoperability for Microwave access*

SUMMARY

Main trends in mobile communication systems are high integration and low power consumption with scaling down to deep submicron, higher data rate with complex and advanced modulation schemes to increase spectrum efficiency, and multiple-standard services. However, as the scaling down is accelerated, the design of a RF PLL as a frequency synthesizer is becoming a more challenging task because of the dynamic range reduction in analog and RF circuits.

The objective of this research is to demonstrate the feasibility of the implementation of wideband RF CMOS PLLs with high spectral purity using deep sub-micron technologies. To achieve wide frequency coverage, this dissertation proposed a 45-nm SOI-CMOS RF PLL with a wide frequency range to support multiple standards. The PLL has small parasitic capacitance with the help of a SOI technology, increasing the frequency tuning range of a capacitor bank. A designed and fabricated chip demonstrates the PLL supporting almost all cellular standards with a single PLL. This dissertation also proposed a third order sample-hold loop filter with two MOS switches for high spectral purity. Sample-hold operation improves in-band and out-of-band phase noise performance simultaneously in RF PLLs. By controlling the size of the MOS switches and control time, the nonideal effects of the MOS switches are minimized. The sample-hold loop filter is implemented within a 45-nm RF PLL and the performance is evaluated. Thus, this research provides a solution for wideband CMOS frequency synthesizers for multi-band, multi-mode, and multiple-standard applications in deep sub-micron technologies.

CHAPTER 1

INTRODUCTION

1.1. Trends of Mobile Communication Systems

The rapid development of wireless communication technology has changed our life styles dramatically over the past twenty years. Even in the middle of the 1980s, the public was not allowed to use or access the wireless network; but now, everyone has his or her own cell phone and can enjoy, with the help of wireless devices, wireless Internet service everywhere. In addition, a car navigation system using a *Global Positioning System* (GPS) instead of carrying paper maps is a basic necessity in our daily lives.

The benefits of *Complementary Metal-Oxide-Semiconductor* (CMOS) technology such as low cost and high-integration capability make it easy to realize small size and lightweight terminals for easy mobility, accelerating the growth of mobile handset market. As the number of consumer increases, the demand for advanced mobile devices, providing not only basic voice communication, but also multimedia data communication services, is growing faster than ever before. Led by this trend, the cell phone has become a handheld computer called “Smartphone”. This device possesses large *Liquid Crystal Display* (LCD) screens, camera modules, *Moving Picture experts group layer-3* (MP3) players, *Universal Serial Bus* (USB) memories, and even mobile processors for real-time data processing. As shown in Figure 1.1, the market growth of Smartphone has outpaced the other mobile phone market [1].

Since data communication is in the forefront of every consumer’s mind, higher data rate has become the first requirement of new emerging standards. Figure 1.2 shows

the evolution of wireless communication standards and peak data-transmission rates [1]. To increase the spectral efficiency of *Radio Frequency* (RF) signals, both phase- and amplitude-modulated signals such as *Orthogonal Frequency Division Multiplexing* (OFDM) signals with high *Peak-to-Average-Power Ratio* (PAPR) are employed for *Long- Term Evolution* (LTE), the pre-fourth generation of cellular wireless standard [2]. High data rate modulation schemes require high spectral purity signals due to the reduced phase error tolerance. Figure 1.3 shows constellations and tolerable phase errors of three phase modulation schemes – *Binary Phase Shift Keying* (BPSK), *Quadrature Phase Shift Keying* (QPSK), 8-PSK. As the spectral efficiency increases, the maximum allowable phase errors decrease.

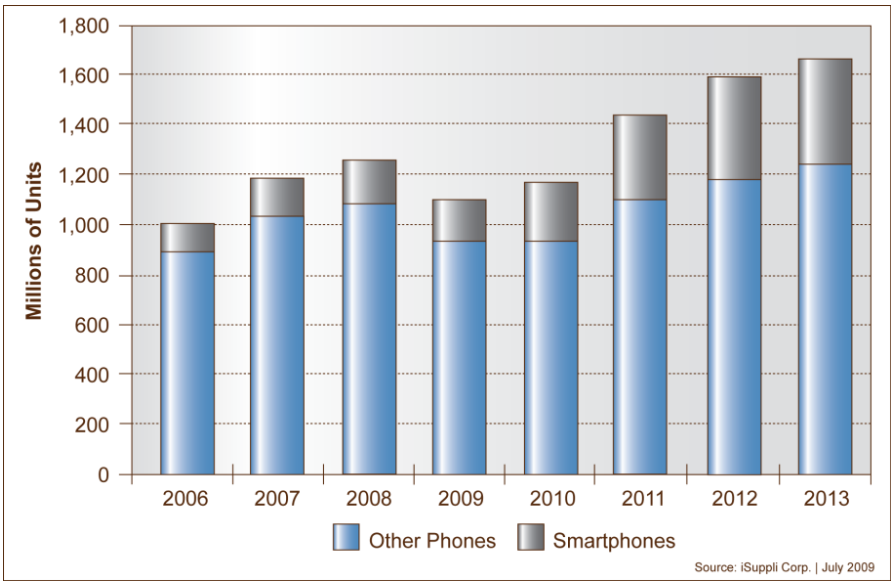


Figure 1.1. Worldwide mobile phone production (Source : iSuppli Corp.).

To incorporate versatile functions in a compact handset, a higher integration level is required. Low power consumption to prolong the battery life is also important for

advanced wireless terminals because handsets need to have sufficient power to run the variety of chipsets for multimedia services and even mobile *Central Processing Unit* (CPU) to deal with increased real time data.

As a result of the scaling down of CMOS technology, low-power baseband and transceiver chipsets have been introduced. Figure 1.4 shows multimedia chipsets in a smart phone [3]. A number of different chipsets are integrated within a small area. To support multiple standards, four *Power Amplifiers* (PAs) are used, while only one transceiver is exploited. This means the single transceiver has to support four different modes.

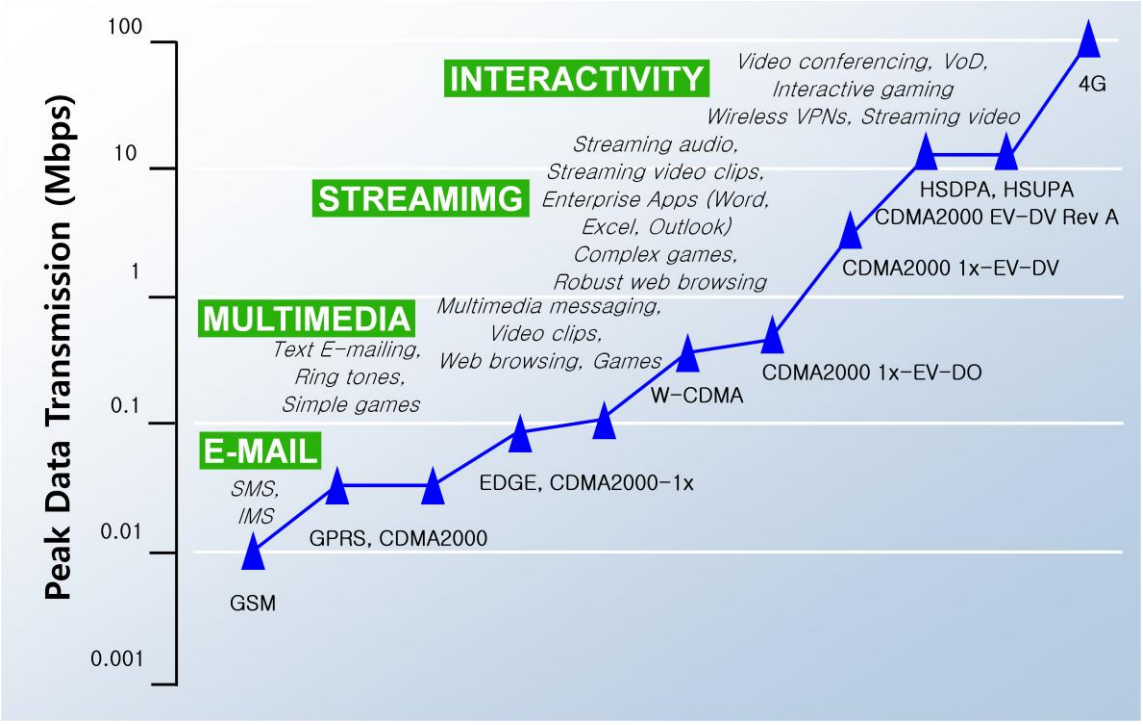


Figure 1.2. Evolution of the wireless communication standards and peak data transmission rates (Source : iSuppli Corp.).

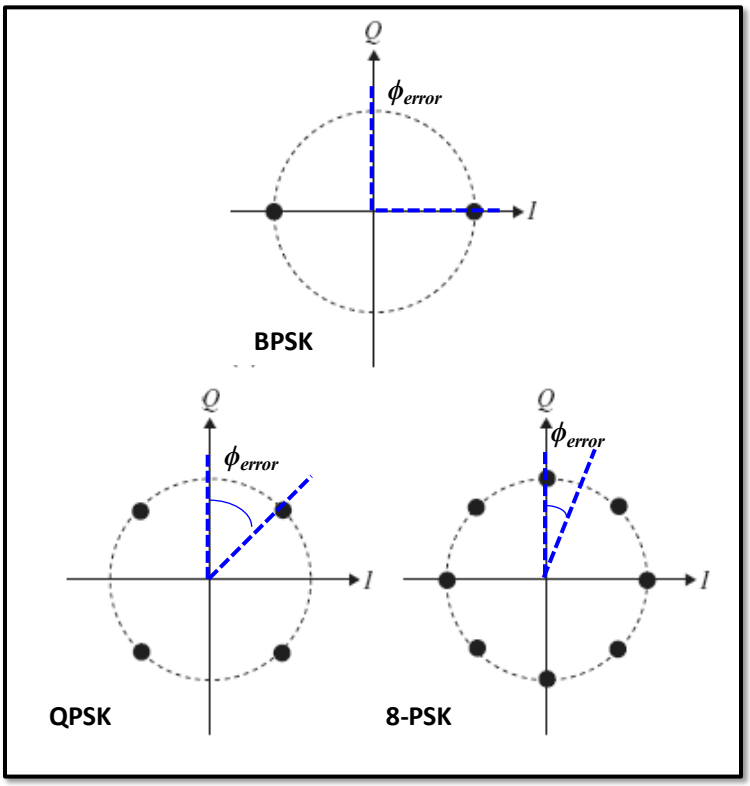


Figure 1.3. Constellation and tolerable phase errors of BPSK (a), QPSK (b), and 8-PSK (c).

Multi-mode and multi-band mobile devices support two or more standards such as *Global Systems for Mobile communications* (GSM), *Code Division Multiple Access* (CDMA), *Enhanced data rates for GSM evolution* (EDGE), *Wideband CDMA* (WCDMA), *Wireless Local Area Network* (WLAN), *Worldwide interoperability for Microwave access* (WiMax), *High Speed Packet Access* (HSPA), and LTE for general-purpose use and backward compatibility with a single package. A *Frequency Synthesizer* (FS), one of the most important blocks in the RF transceiver, generates the carriers for *Transmission* (Tx) and the LO signals for *Reception* (Rx). Since the spectral purity of RF signals is directly affected by the FS, the performance of the FS is critical to the overall system performance. A multiple-standard-supporting transceiver is shown in Figure 1.5.

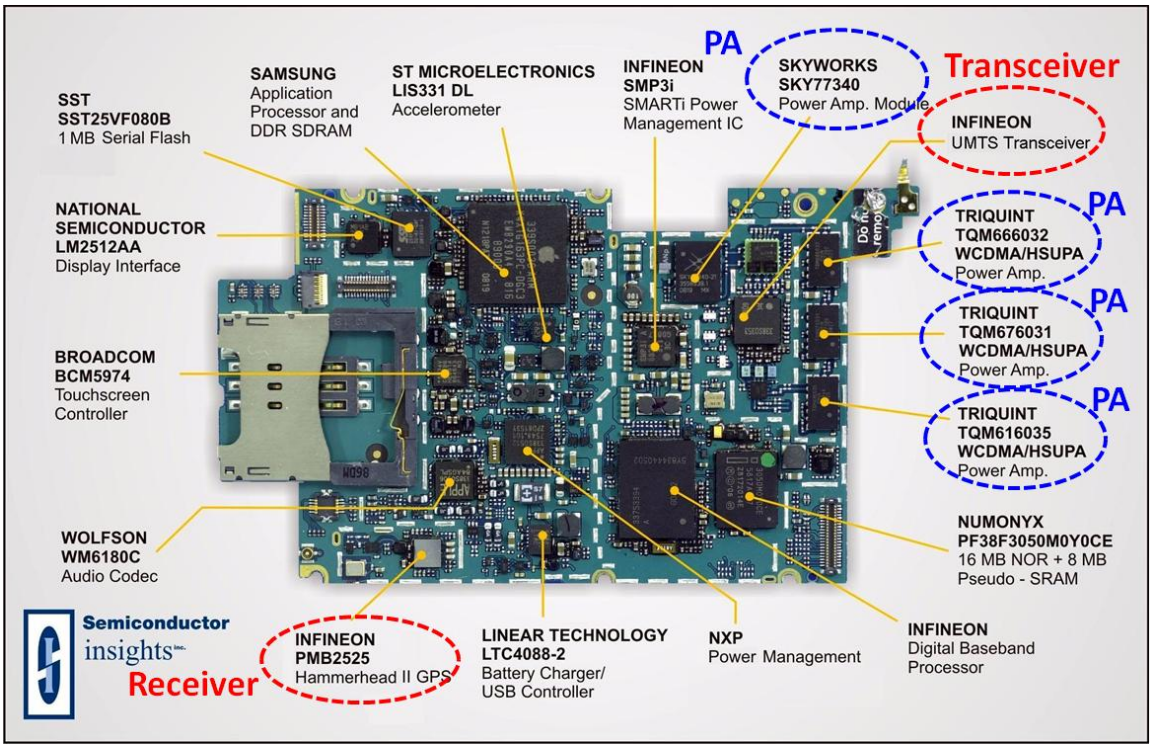


Figure 1.4. Multimedia chipsets in Smart Phone - iPhone3
(Source : Semiconductor insights Corp.).

Even though the transceiver is supporting multiple-modes, multiple-bands such as UMTS, HSDPA, HSUPA, and EGPRS (EDGE/GPRS/ GSM), only two or three FSs are integrated within the chips. Each FS has to support multiple modes and multiple bands of different standards with a very wide frequency range. Moreover, the FS has to support both Rx and Tx modes with a single *Voltage-Controlled Oscillator* (VCO) when the standard uses *Time Division Multiple Access* (TDMA) principles like GSM and EDGE. Therefore, the FS has to meet all specifications of the standards at the same time. Accordingly, the design of FSs satisfying these is a very challenging task.

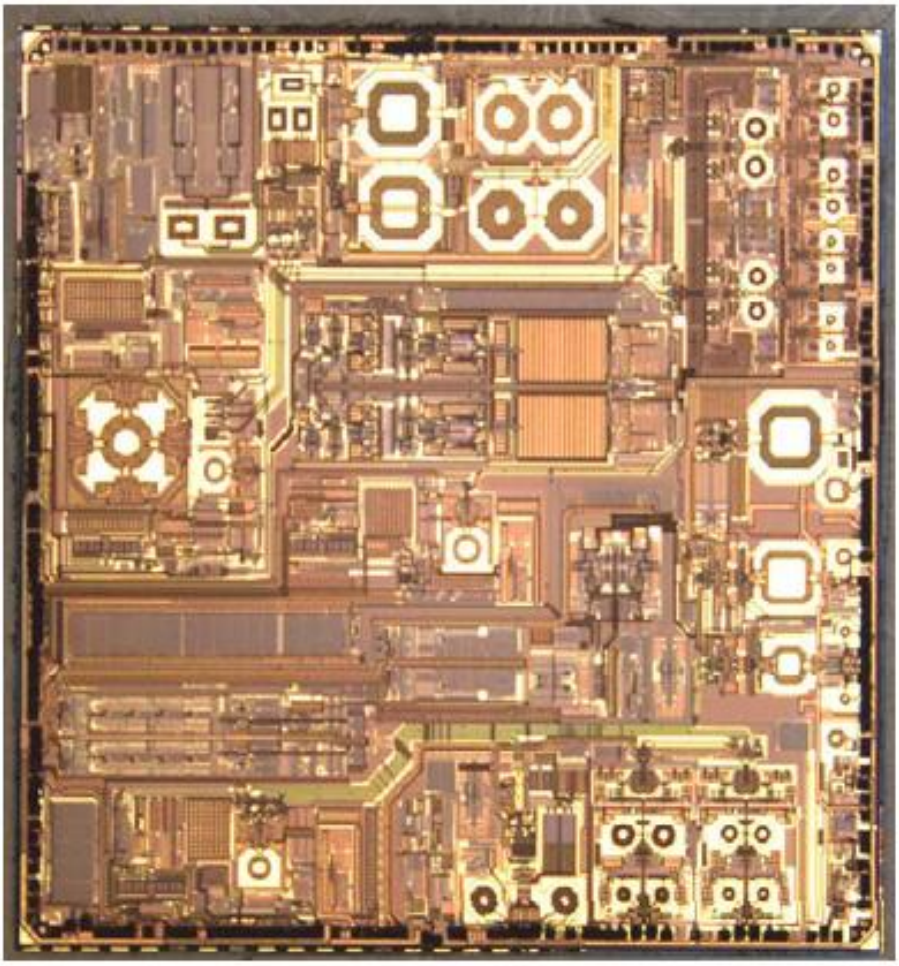


Figure 1.5. Multiple-standard-supporting transceiver (Qualcomm Transceiver RTR6285).

Table 1.1 shows the frequency allocations for various standards for mobile communication systems. Oscillation frequencies of more than 5 GHz with frequency coverage of more than 67% are required with a single VCO to support all standards listed in Table 1.1. But, due to large parasitic capacitance and low *Quality-factor* (Q-factor) of passive components, the implementation of high-quality and high-frequency LC-VCOs with a wide-tuning range is also a challenging task in standard bulk CMOS technologies.

Table 1.1 Frequency allocations for some wireless applications.

Application	Standard	E-UTRA Bands for LTE	Frequency (MHz)
Cellular	GSM 850		824~894
	E-GSM 900		880~960
	DCS 1800		1710~1880
	PCS 1900		1850~1990
	CDMA (IS-95)		824~894 1850~1990
	USPCS		1850~1995
	LTE	5,6,8,13,14	746~960
		11	1428~1500
		1~4,9,10,33~37,39,40	1710~2400
		7,38	2500~2690
WLAN	IEEE 802.11a/n		5150~5825
	IEEE 802.11b/g/n		2400~2497
WiMAX	IEEE 802.16 e		2300~2700
	IEEE 802.16 e/d		3300~3800
	IEEE 802.16 e/d		5150~5850

1.2. Thesis Organization

As shown in the previous section, the main trends in mobile communication systems are high integration and low power consumption with scaling down to deep submicron, higher data rate with complex and advanced modulation scheme to increase spectrum efficiency such as OFDM and 64 *Quadrature Amplitude Modulation* (QAM), and multiple-standard services.

There are trade-offs between two trends as shown in Figure 1.6. The final goal of this research is to develop a wideband *Phase-Locked Loop* (PLL) with high spectral purity for wireless communication systems. Since a *Charge-Pump* (CP) PLL has been a general form in frequency synthesis, the issues of CPPLLs and issues coming from the scaling down of CMOS technologies are focused on in this thesis. The first goal of this

work is to overcome the inherent drawbacks of CPPLLs so that the CPPLLs can improve spectral purity to meet the specifications of various standards. The second goal is to design a CMOS PLL with a very wide frequency range to support multi modes, multi bands, and multi standards with a single VCO.

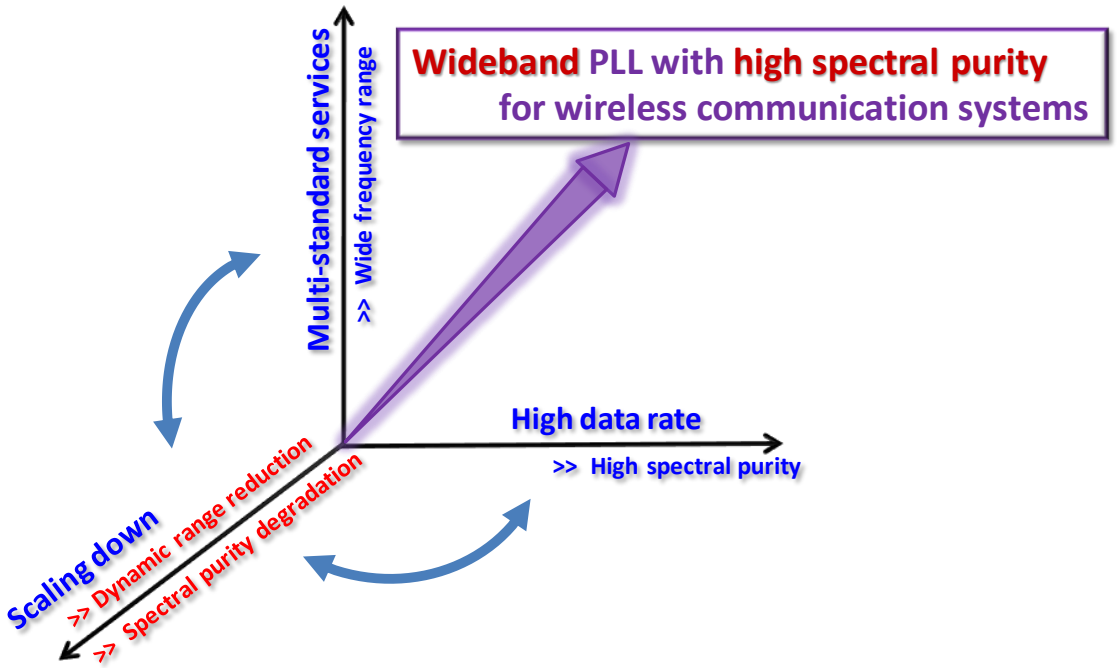


Figure 1.6. Trends of wireless communication systems and design goal of this research.

This dissertation consists of seven different parts. Chapter 2 presents general architectures of transmitters for mobile communication systems to get the big picture and the role of each block in transmitters. PLL is a main key block in transmitters, so the basic operation and main issues are explained. In Chapter 3, generic PLL operation and the design issues of sub-blocks are analyzed are presented. Chapter 4 gives a detail explanation about challenges in charge-pump PLL design. There are many design issues when CPPLLs are designed such as *Phase Frequency Detector* (PFD)/CP linearity,

Delta-Sigma Modulator (DSM) noise boosting in out-of-band, bulky *Low Pass Filter* (LPF) size, and continuous up and down current pulses. One more issue we have to consider is the performance limitation coming from scaling down to deep submicron. As the solution of the first goal, a third order sample-hold loop filter is introduced in Chapter 5. Comparison with prior arts, circuit design, analysis, and measurement results are presented in detail. In Chapter 6, a fully integrated wideband PLL is proposed. The PLL incorporates the third order sample-hold loop filter presented in Chapter 5 for high spectral purity. To maximize the frequency range, a SOI-CMOS process is adopted. Each block design and measured results of a fabricated chip are described. Finally, Chapter 7 concludes and summarizes the work done with this thesis.

CHAPTER 2

TRANSMITTERS FOR MOBILE COMMUNICATION SYSTEMS

2.1. Architectures

A representative architecture for transmitters is direct conversion type [4]. The upper part of Figure 2.1 illustrates this. In direct-conversion architecture, baseband modem generates *Inphase and Quadrature* (I/Q) signals from a single modulated signal. The separated I/Q signals are converted to the analog domain using *Digital-to-Analog Convertors* (DACs) and combined after mixers. A *Local Oscillator* (LO) generates fixed carrier frequencies and Mixers convey the baseband signals to the carrier frequencies. The combined signal is followed by *Surface Acoustic Wave* (SAW) filter and is transferred to the PA for transmission. The merit of this architecture is that there is no data rate limit in the input modulated signal, so high data rate signals can be upconverted without any bandwidth limitation. However, the hardware complexity is high because of mixers for upconversion of baseband signals, an I/Q signal generator for the LO signal, and an I/Q signal combiner before a driver amplifier. Since I/Q mismatch and DC offset degrade the performance of the transmitters, external bulky SAW filters are usually employed.

Simple PLL-based transmitters have much benefit in hardware complexity as shown in the lower part of Figure 2.1 [5]. Even though a *COordinate Rotation DIgital Computer* (CORDIC) block as a Cartesian-to-polar converter is required [6], it is realized in digital domain so the burden in circuit design is not high. Operation is follows. The baseband I/Q signals are converted to a polar form, consisting of phase- and

amplitude-modulated signals. The phase-modulated signal is transferred to a PLL and the PLL becomes a phase/frequency modulator. When a new phase-modulated signal is applied to a fractional engine such as a DSM, PLL generates modulated RF signals without mixers or I/Q generators. The amplitude-modulated signal is transferred through separate paths and combined in a driver or a PA. With this approach, many RF blocks are saved with smaller power consumption. Since the delay difference between two paths can degrade the *Error Vector Magnitude* (EVM) performance, a careful delay control is essential in this architecture.

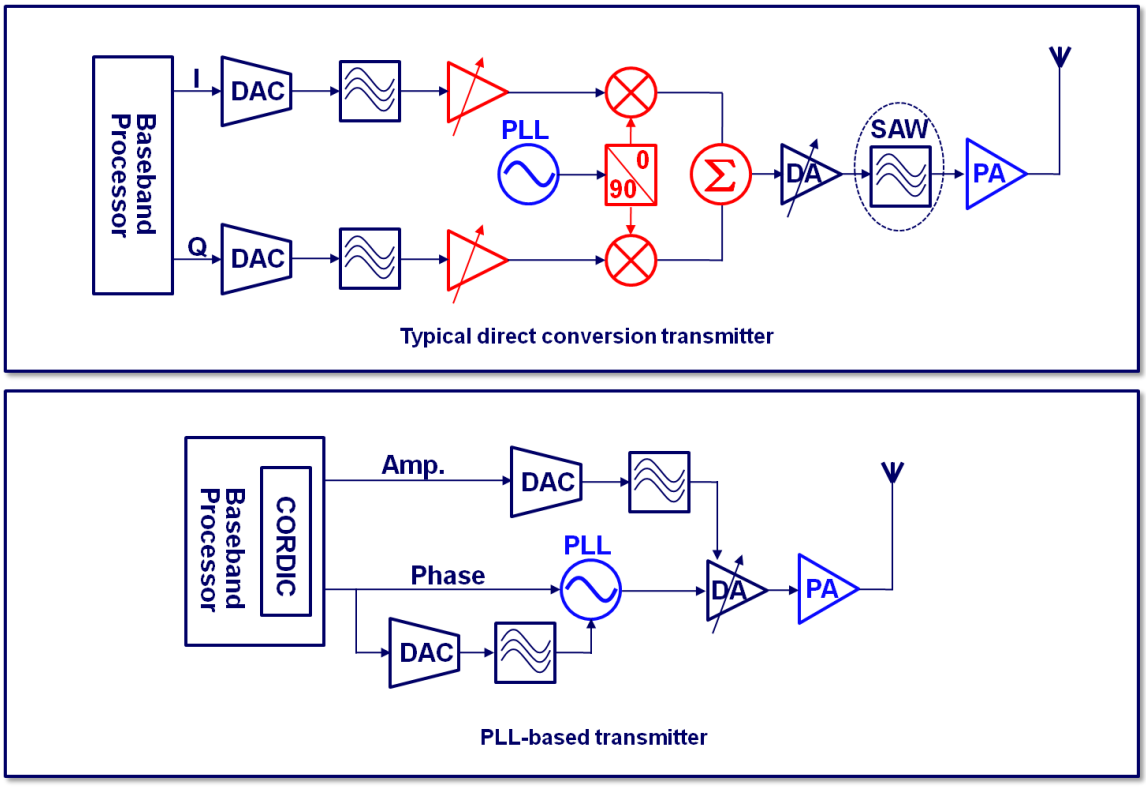


Figure 2.1. Typical architectures of transmitters for mobile communication systems. Direct conversion and PLL-based transmitters.

PLL-based transmitters have gained popularity because of the direct modulation capability of VCOs with accurate frequency control as well as the simplicity in architecture. In both architectures, the common key RF blocks are PLLs and PAs. Since the main topic of this thesis is PLLs, the design concerns and the roles of PLLs in transceivers are discussed in the following section.

2.2. Phase-Locked Loop in Direct Conversion Transmitters

Even though PLLs are commonly used in two transmitter architectures, the expected roles and required key performances are different. In the direct conversion architecture, the PLL generates LO signals and followed by an I/Q signal generator. So it is a PLL-based frequency synthesizer. The input of the PLL is just fixed channel frequencies as shown in Figure 2.2. A reference signal is generated from a *Digitally Controlled Crystal Oscillator* (DCXO) or an external *Voltage Controlled- Temperature Compensated Oscillator* (VC-TCXO). Main specifications are phase noise and low spurious tone level. In-band phase noise level is important because it, along with I/Q signal mismatch, is directly related to the *Root Mean Square* (RMS) phase error in constant envelop modulation scheme like GSM and EVM in phase and amplitude modulation schemes, such as WCDMA and EDGE. Out-of-band phase noise and spurious tones are also critical when blockers exist. High out-of-band phase nose level results in fail to meet output RF spectrum requirement. To be well confined within the mask specification lines, high spectral purity is essential, which has low phase noise and small spurious tone levels. Wide frequency range is another important requirement because a single FS has to support multi bands, multi modes, and multi standards.

2.3. Phase-Locked Loop in PLL-based Transmitters

On the contrary, PLLs in PLL-based transmitters generate modulated RF signals instead of single tones, and they become PLL-based phase/frequency modulators. The inputs of the PLLs are mixtures of channel frequencies and modulation data in frequency domain. However, as the demand for higher data rate increases, the PLLs present a problem when designing the PLL-based phase/frequency modulators since the data rate becomes higher than the PLL bandwidth. PLLs do not response to the higher frequency signals than the PLL bandwidth owing to its low-pass filtering characteristic. To overcome this challenge, a two-point modulation scheme is generally adopted [7]. It effectively expands the signal bandwidth by applying the modulation signals at two different points as shown in Figure 2.3. The low-frequency portion of the signals is modulated through the PLL loop and the high-frequency portion is by the VCO. As a result, the recombined signals show all-pass filtering properties without being restricted by the PLL bandwidth. Figure 2.4 shows the modulation response of a typical two-point modulator.

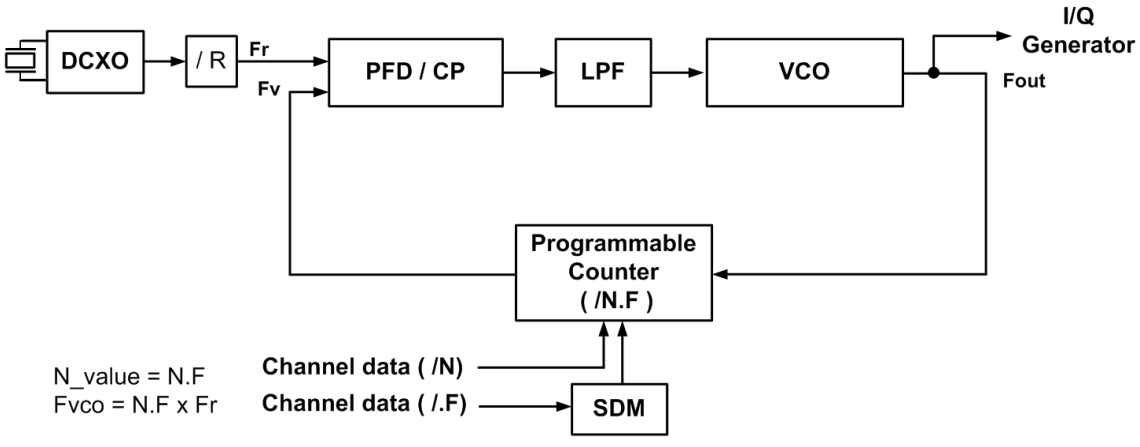


Figure 2.2. PLL-based frequency synthesizer in a direct conversion transmitter.

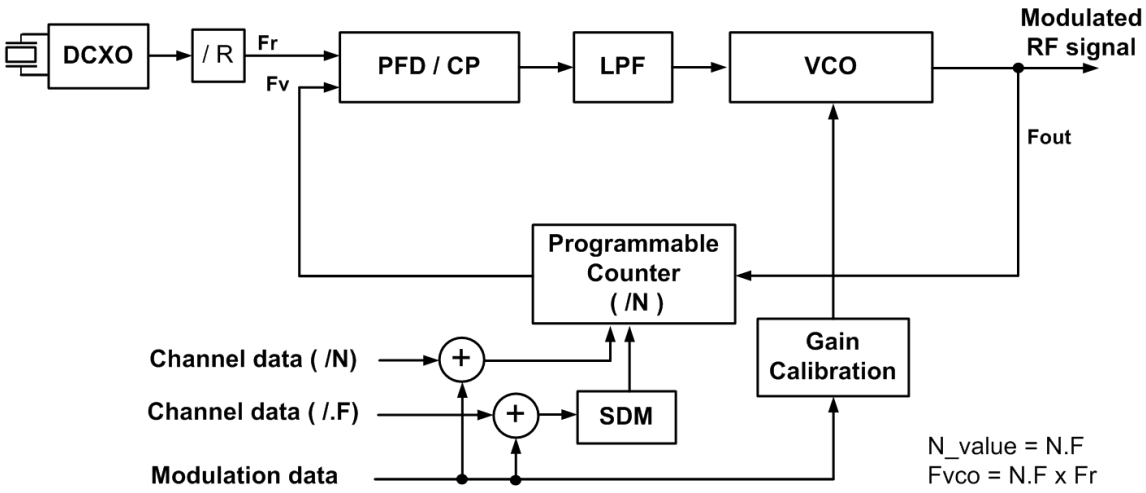


Figure 2.3. PLL-based phase/frequency modulator in a PLL-based transmitter.

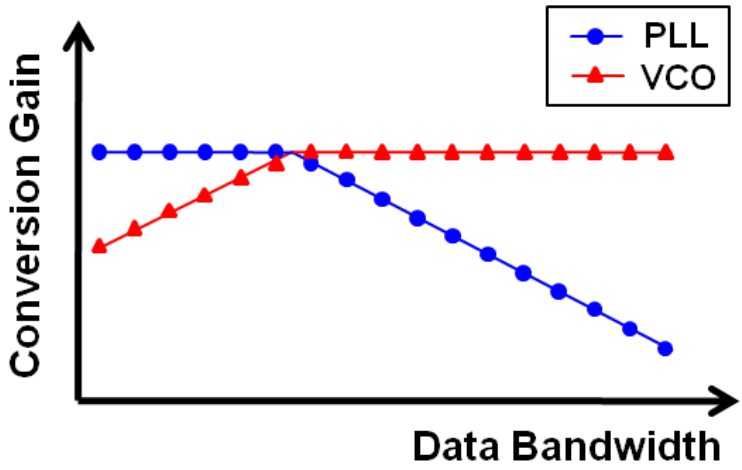


Figure 2.4. Modulation response of a typical two-point modulator.

Since there are two signal paths, the delay mismatch between two paths can degrades RMS phase error or EVM performance. Figure 2.5 shows peak and RMS phase errors of a two-point modulator when a GSMK modulation signal is applied for GSM application. The delay mismatch should be less than 0.5 of the system clock period for

the performance not to be degraded. The gain mismatch between two signal paths also degrades the performance of the two-point modulator as shown in Figure 2.6.

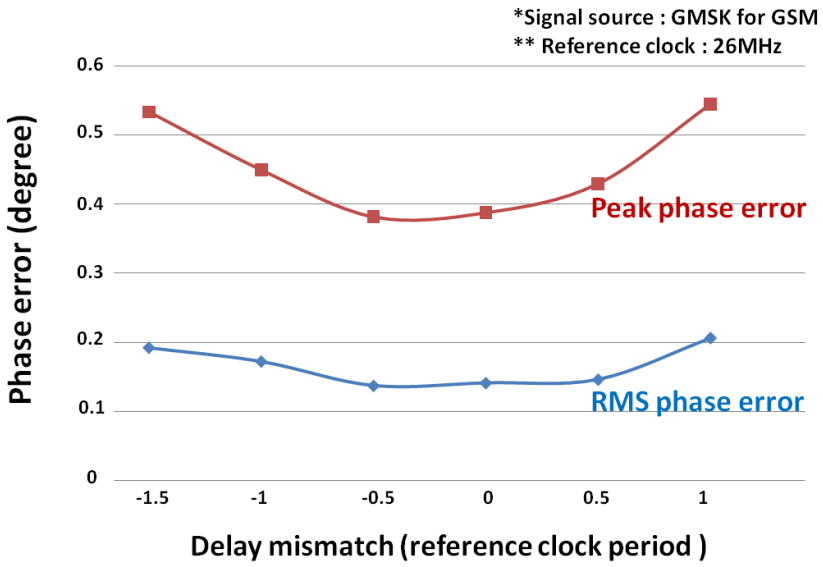


Figure 2.5. Phase error depending on delay mismatch between two signal paths in a PLL-based two-point modulator when a GSMK modulation signal is applied for GSM application.

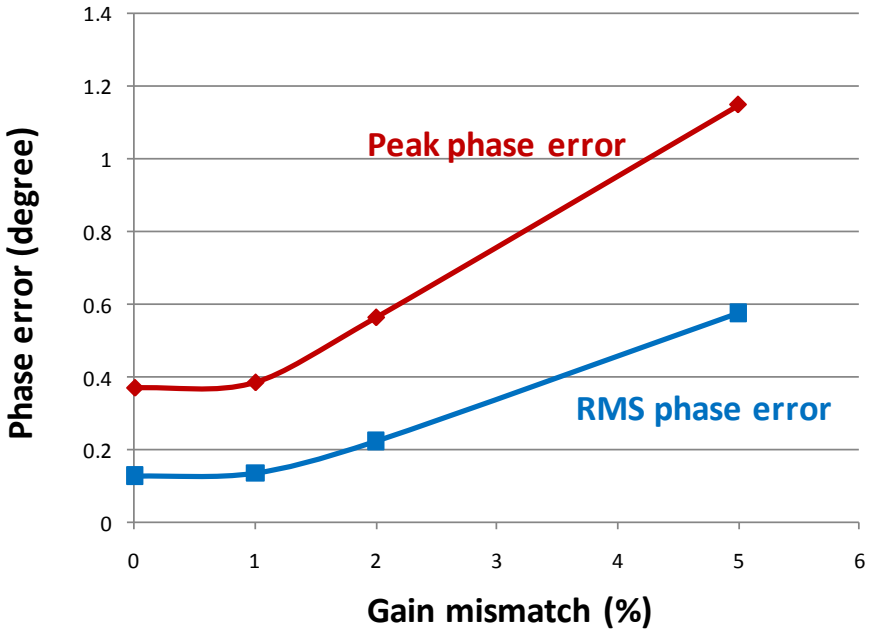


Figure 2.6. Phase error depending on gain mismatch between two signal paths in a PLL-based two-point modulator when a GSMK modulation signal is applied for GSM application.

Total lock time is also a major issue in two-point modulator because another gain calibration time is required as shown in Figure 2.7. Generally, the gain calibration time is inversely proportional to the gain error. The gain calibration time to obtain less than 1% gain mismatch is comparable to the PLL settling time. Moreover, since a pilot signal is applied to the modulator during gain calibration, another PLL settling time is required for phase lock when the pilot signal is removed after gain calibration [8].

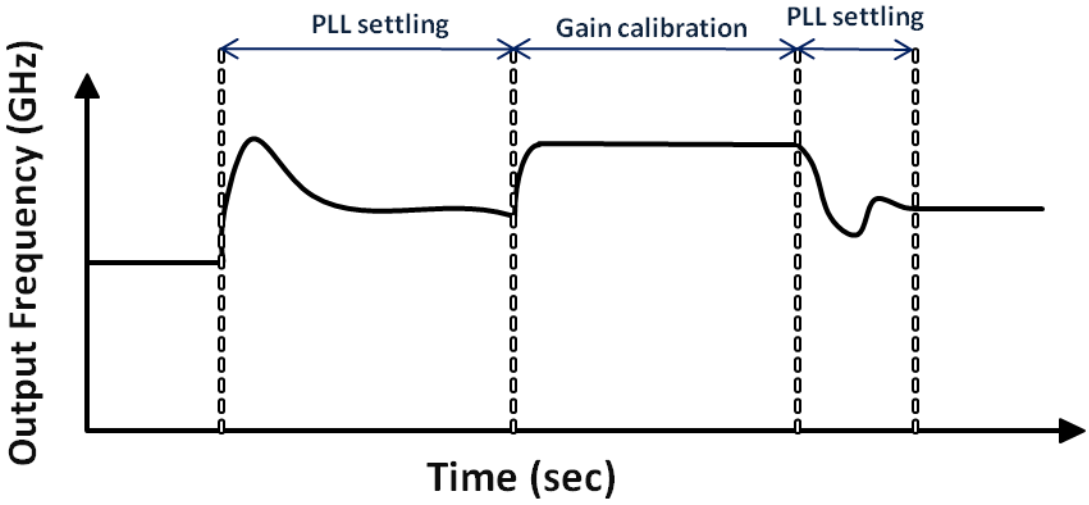


Figure 2.7. Locking process of a two-point modulator. Another gain calibration time is required.

CHAPTER 3

CHARGE-PUMP PHASE-LOCKED LOOP

3.1. Basic Operation of Charge-Pump Phase-Locked Loop

A PLL is a feedback system, generating fixed frequencies from a fine reference signal. A VCO output is divided down to a feedback signal. The reference and the feedback signals are compared each other, and the error between two signals controls the next feedback signal and system output. Therefore, several blocks within the system should be well organized to be stable and to generate high spectral purity signals. A traditional PLL has a phase detector or a frequency detector or both of them, so phase difference is diminished through a phase detector path and frequency deviation is reduced using a frequency detector path. Since frequency locking range is limited within a finite range, if the frequency difference is too much large, the PLL fails to lock to the requested frequencies. Another drawback is that a 180-degree static phase offset or finite phase error exist even when the PLL is in locked condition.

However, a CPPLL detects both phase and frequency difference between two input signals at the same time with a PFD block. Moreover, it has an infinite gain for a static phase difference, providing infinite frequency resolution, and the capture range is not limited if the VCO tuning voltage is not limited by supply voltage. Therefore, a CPPLLs has become the most general form for frequency synthesis. A CPPLL consists of a VCO as a output signal generator, a divider as a frequency down-converter in the feedback path, a PFD for input signal comparison, a CP, and a LPF for current-to-voltage conversion. Figure 3.1 shows a simplified block diagram of a CPPLL. Generally, the

output frequency is higher than the reference frequency since it is multiplied by dividing value, *N*. The two input signals will have the same frequency when the PLL finishes the locking process. Therefore, the output frequency, F_{vco}, is defined by following equation, where the F_r and F_v are the frequencies of reference and feedback signals, respectively.

$$F_{vco} = F_v \cdot \mathrm{N} \approx F_r \cdot \mathrm{N} \quad (1)$$

The operation of the PLL is as follows. When a new VCO output frequency is requested, the VCO has an initial tuning voltage and an initial output frequency. The initial output frequency is divided by the divider in the feedback path, and it is fed back to the PFD as one input. The other input comes from a reference clock generator. Two input signals are compared in the PFD. The PFD converts the frequency and phase difference between two input signals to phase difference. The PFD derives the CP with its output signals, U_p/D_n. The CP becomes a current source or current sinker depending on the U_p/D_n signals. The phase difference information is converted to up and down currents in the CP output. Since the CP generates continuous current pulse train, the LPF is required to smooth it out. The LPF also has a role as a current-to-voltage converter because the VCO is controlled by a tuning voltage. The VCO output frequency changes in accordance with the tuning voltage. This operation continues until the loop is settle down to a stable condition and PLL goes into a locked condition.

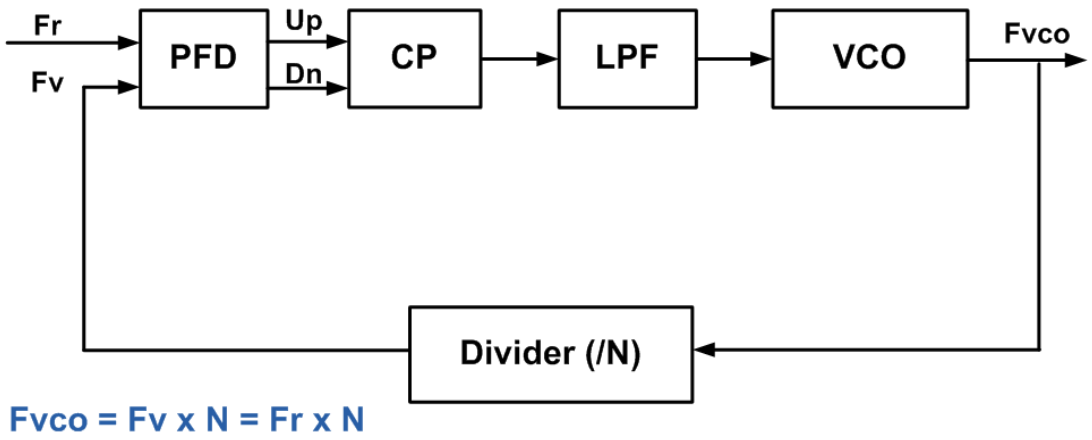


Figure 3.1. Simplified block diagram of a CPPLL.

3.2. Architectures

There are two different architectures in CPPLLs; an *IN-PLL* (IN-PLL) and a *Fractional-N PLL* (FN-PLL). The IN-PLL generates integer-multiple frequencies of the reference signal as outputs, thus the frequency of the reference signal determines the frequency resolution of the output signals. To realize a fine frequency resolution in the VCO output, a lower frequency signal should be used as a reference signal. However, important characteristics such as PLL loop bandwidth, locking time and, in-band phase noise are limited by this.

FN-PLL has one more degree of freedom in choosing the frequency of the reference signal because it provides continuous output frequency independent of the frequency of the reference signal. In a FN-PLL, a fractional engine is added to the IN PLL. The engine changes the dividing value of the feedback signal instantaneously but the average dividing value converges to a requested fractional dividing value. Since the

advantage of continues frequency generation, the FN-PLL is more prevalent in mobile communication systems. More detail explanation will be followed.

3.2.1 Integer-N PLL

The block diagram of an IN-PLL is shown in Figure 3.1. As mentioned before, the IN-PLL has an inherent drawback in choosing the frequency of the reference signals. With the IN-PLL, the frequency of reference signal should be less than the channel spacing of a system. For example, the frequency difference between adjacent channels is 200 KHz in GSM systems, thus the reference frequency should be 200 KHz at most [9][10]. When we use low reference frequency signals, there are four issues coming from it.

The first one is locking time. The PLL loop bandwidth is limited by the frequency of the reference signal because of stability issue. The following equation is derived by Gardner in a CPPLL with a simple LPF as shown in Figure 3.2, where I_{cp} and K_{vco} are CP current and VCO gain, respectively [11].

$$\omega_n{}^2 = \frac{\omega_r{}^2}{\pi(RC \cdot \omega_r + \pi)}, \quad \omega_r = 2\pi f_r \tag{2}$$

The natural frequency of the PLL, ω_n, is limited by the reference frequency, f_r. The rule of thumb in typical PLL design is that the PLL bandwidth should be less than one-tenth of the input signal frequency [12]. Small bandwidth results in longer locking time.

The second one is in-band phase noise degradation due to large dividing values. In mobile communication systems, the output frequency range reaches from 800MHz to more than 2GHz. If the output frequency is 800MHz with a reference frequency of 200 KHz, the dividing value is 4000. Since in-band noise voltage is multiplied by the dividing ratio at the output of PLL, in-band phase noise, $L(\omega)$, is multiplied by the square of the dividing values as shown in equation (3).

$$\overline{v_{noise\_out}} \propto 10 \cdot \log |\mathrm{N}| \tag{3}$$

$$L(\omega) \propto 20 \cdot \log |\mathrm{N}| \tag{4}$$

It is clear with this equation that the large dividing ratio to generate the same output frequency degrades the in-band phase noise performance in PLLs.

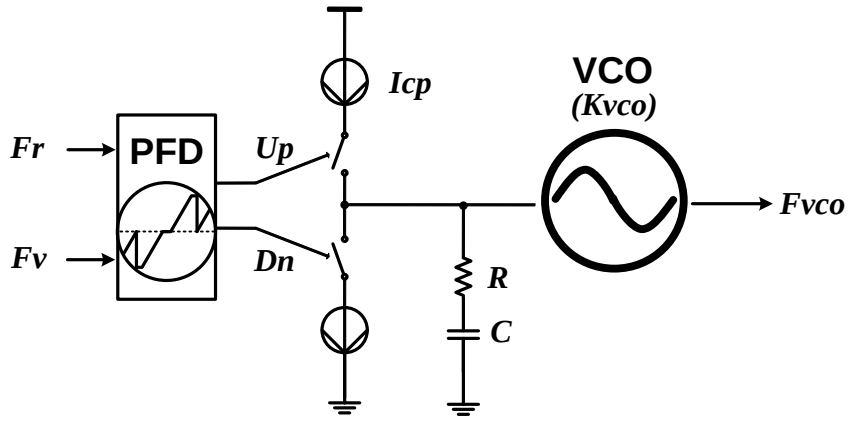


Figure 3.2. Simplified block diagram of a CPPLL for calculation of bandwidth limitation.

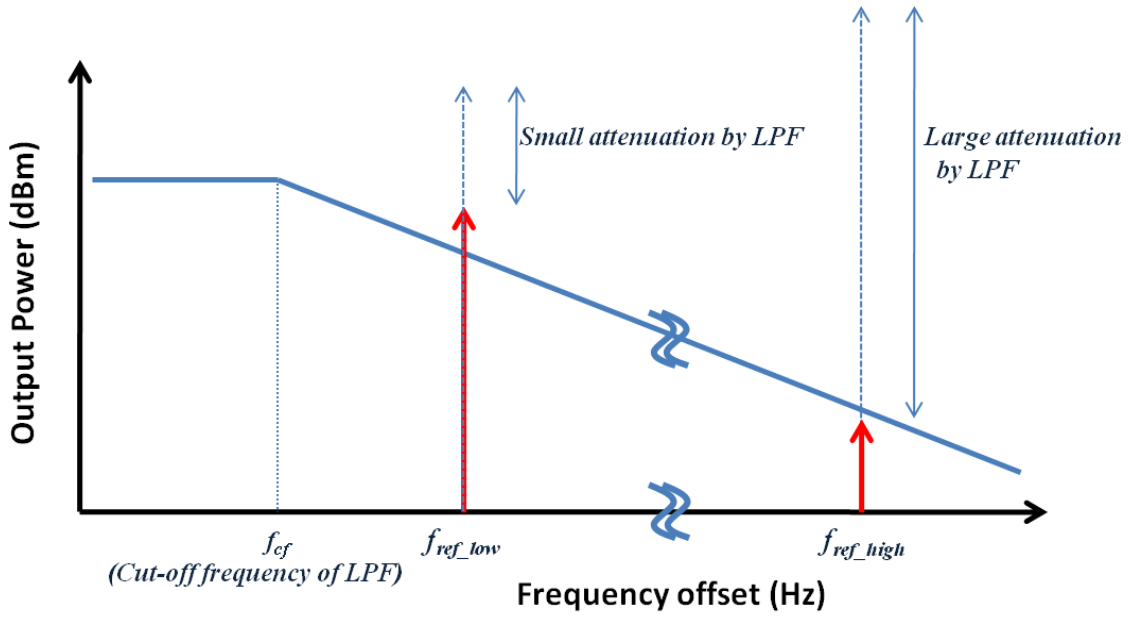


Figure 3.3. Reference spur level depending on the cutoff frequency of a LPF and the frequencies of a reference signal.

The third negative aspect with low reference frequency is higher reference spur level due to small frequency distance between the cut-off frequency of the LPF and the reference frequency. To clarify this, let's consider a PLL with different reference frequencies but with the same cut-off frequency of the LPF, f_{cf}, as shown in Figure 3.3. The reference spur level of the signal with lower frequency, f_{ref_low}, is less attenuated by the LPF than the reference signal with higher frequency, f_{ref_high}. Spur level is attenuated depending on the offset frequency between f_{cf} and the reference frequency, f_r. If the PLL employs a N^{th}-order LPF, the attenuation factor is defined by

$$\alpha = 20 \cdot \mathrm{N} \cdot \log\left(\frac{f_{cf}}{f_r}\right). \qquad (f_{cf} \ll f_r) \tag{5}$$

In the FN-PLL, the frequency of the reference signal can be increased to more than 100 times of the value of IN-PLL. Therefore, the reference spurs can be attenuated to very small levels.

The last one is the effect of leakage current. If there is a static leakage current, the tuning voltage change due to the leakage current is much higher with a low reference frequency signal than that with a high reference frequency signal. Figure 3.4 illustrates the model of a CPPLL with a static leakage current, $I_{leakage}$. The tuning voltage fluctuation due to the static leakage current, $\Delta V_{leakage}$, is described in Figure 3.5. The fluctuation voltage is given by

$$\Delta V_{leakage} = \frac{I_{leakage} \cdot T}{C} \tag{6}$$

, where T is the period of the reference signal. To reduce $\Delta V_{leakage}$, the frequency of the reference signal should be incrassated or a larger zero-making capacitor is required. The PLL with a leakage current will compensate the charge loss with more charging current under locked condition. The periodic net *up* current increases the reference spur level. The amount of the net *down* current is proportional to the leakage current. The time duration of the net *up* current is

$$\Delta\tau = \frac{I_{leakage} \cdot T}{I_{cp}} . \tag{7}$$

Large CP current also lessens the effect of the leakage current. If we assume the fluctuation of the VCO tuning node results in narrow-band FM modulation, the spur level at VCO output due to static leakage current is

$$Spur_{\_wo\_LPF} = 20 \log \left(\frac{K_{vco} \cdot \Delta V_{leakage}}{2 \cdot f_r} \right). \quad (8)$$

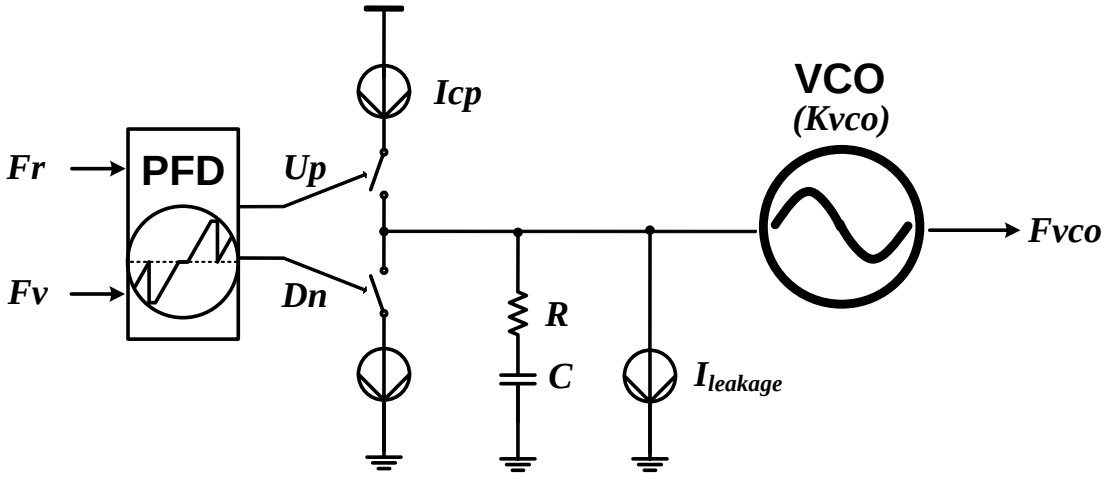


Figure 3.4. Simplified block diagram of a CPPLL with a static leakage current.

If the attenuation by the LPF is considered, the spur level at the VCO output due to the static leakage current will be

$$Spur = \alpha + 20 \log \left(\frac{K_{vco} \cdot \Delta V_{leakage}}{2 \cdot f_r} \right)$$

$$= 20 \cdot N \cdot \log \left(\frac{f_{cf}}{f_r} \right) + 20 \log \left(\frac{K_{vco} \cdot \Delta V_{leakage}}{2 \cdot f_r} \right). \quad (9)$$

Equation (9) also indicates that the spur level can be reduced with higher reference frequency signals.

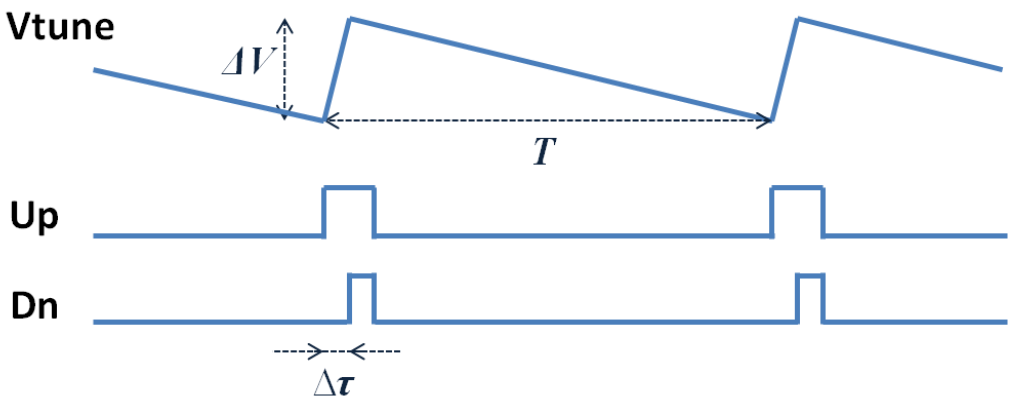


Figure 3.5. Tuning voltage fluctuation and CP output due to a leakage current.

3.2.2 Fractional-N PLL

IN-PLLs have advanced to FN-PLLs to synthesis continuous VCO output frequencies using fractional engines, such as DSMs and accumulators, with a very fine frequency resolution. Figure 3.6 shows an example of a FN-PLL. The fractional engine determines the instantaneous dividing ratio of the feedback signals and enables the average dividing ratio to be a fractional value. So the fractional engine together with the divider becomes a fractional divider as a whole. Figure 3.7 explains how the fractional divider realizes a fractional dividing value. If the target dividing value is *N.2*, the fractional engine generates eight times *N* and two times *N+1* as outputs. In this manner, FN-PLLs can increase the frequency of the reference signal independently on the channel spacing. Accordingly, the PLL loop bandwidth can be also increased. The in-band phase noise has been improved by the reduced small dividing values. And reference spurs are

very well suppressed by the LPFs because of large offset frequencies. Smaller period of the reference signal lowers the effect of the static leakage current. Since an accumulator is used as the fractional engine, the same output pattern is repeated, creating spurious tones. Different to the accumulator, DSMs determine the instantaneous dividing ratio of the feedback signals without any significant periodic tones with the help of their randomizing nature. Led by this advantage, the FN-PLLs with DSMs have been prevalent in the RF transceivers [13].

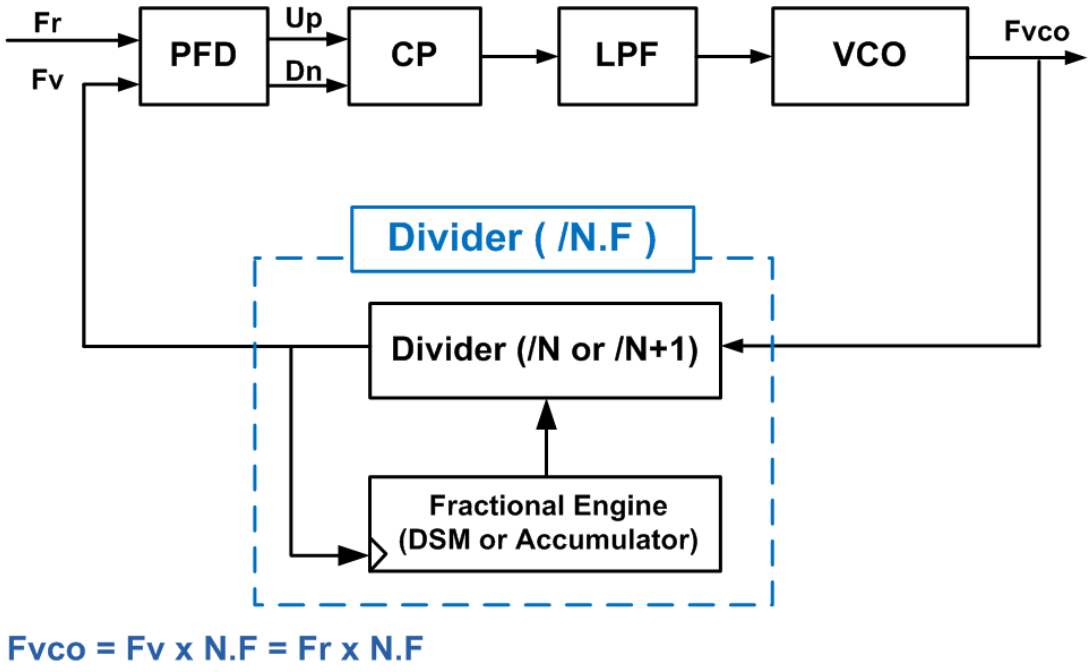


Figure 3.6. Simplified block diagram of a FN-PLL.

However, FN-PLLs suffer from idle tones and fractional spurs. Idle tones, caused by the repeating patterns of DSMs, can be reduced with higher order DSMs or dithering techniques, but the fractional spurs can be problematic because they can be located close to the carriers or within the PLL loop bandwidth, critically deteriorating the spectral

purity. The DSMs also result in negative effects on phase noise. The nonlinearity of the PFD/CP results in the noise-folding effect, folding the high frequency noise of DSMs back into the low frequency band. Even thought DSMs improve the *Signal to Noise Ratio* (SNR) around the carrier frequencies by the noise-shaping effect, pushing noise to higher frequency region, this degrades the out-band phase noise of FS-PLLs if the LPF does not suppress the boosted noise below the noise level of the VCO as shown Figure 3.8 [14]. Increased hardware complexity is another burden in FN-PLLs since the size of DSM is comparable to PFD and CP. The switching noise from the DSM affects other blocks via substrate, and ground and power supply lines.

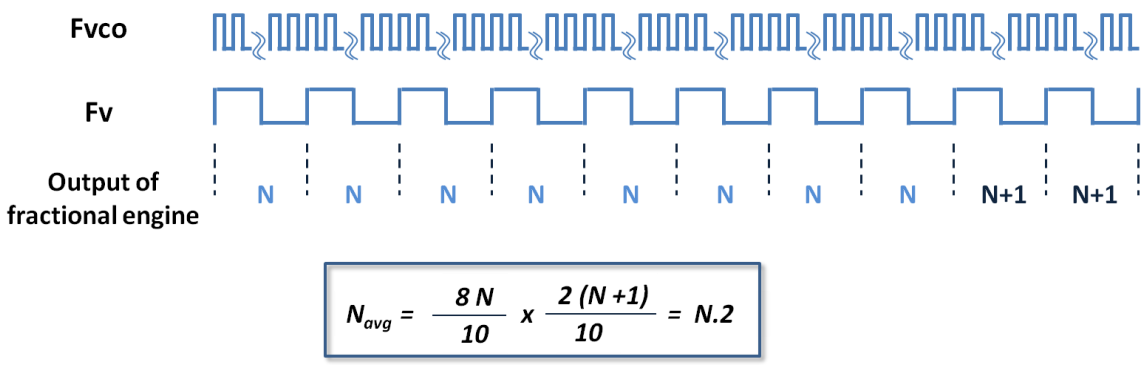


Figure 3.7. Realization of a fractional diving value with an accumulator.

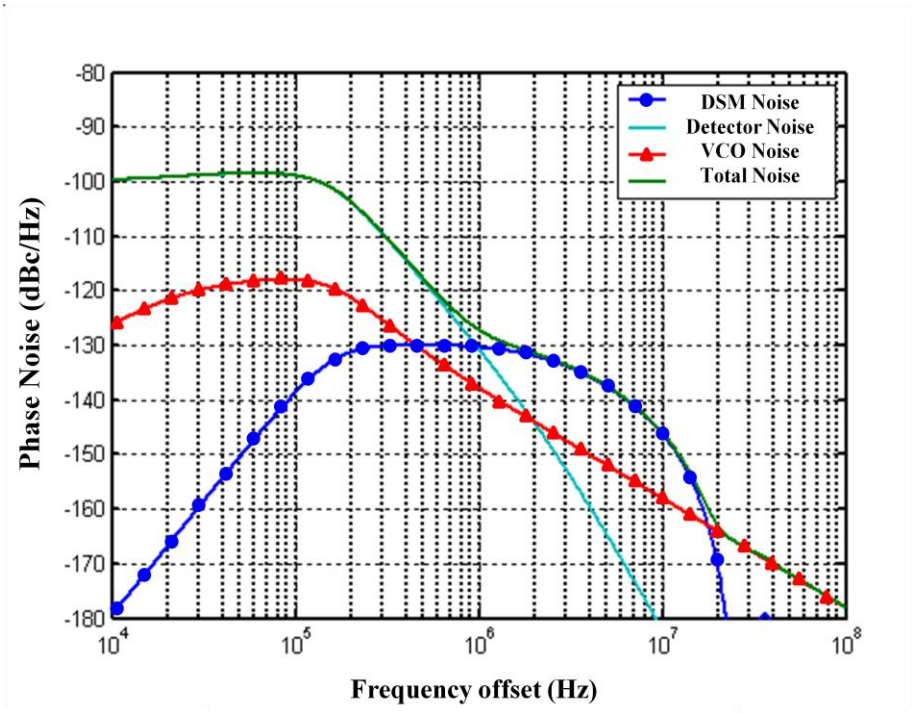


Figure 3.8. Typical phase noise contributions of each component in a FN-PLL.

3.3. Building Blocks

In this chapter, the basic building blocks of the FN-PLLs are discussed. There are seven major blocks in a FN-PLL; VCO, PFD, CP, LPF, DSM, Divider, and Prescaler.

3.3.1. Voltage-Controlled Oscillator

A VCO is a voltage-to-signal generator as shown in Figure 3.9. The output frequency of a VCO is determined by two parts, free running frequency part, f_{free_run}, and excessive frequency part, f_{ex} [15].

$$F_{vco} = f_{free} + f_{ex} = f_{free} + K_{vco} \cdot Vtune \quad (10)$$

The excessive frequency is controlled by the tuning voltage, but the free running frequency is not controllable.

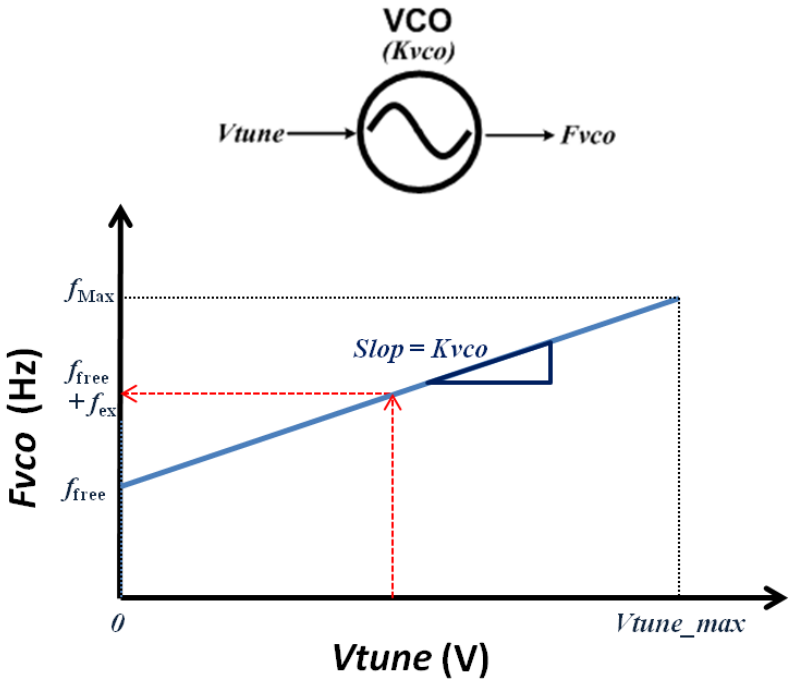


Figure 3.9. Excessive frequency control by the VCO tuning voltage in a FN-PLL.

There are two types of VCOs; LC-VCOs and ring VCOs. In RF systems, LC-VCOs are generally used because of the better phase noise performance than ring VCOs. The LC-tank in a LC-VCO shapes VCO output noise into a very narrow bandwidth and provides high spectral purity. Figure 3.10 shows a typical LC-VCO, consisting of an inductor, a fixed capacitor, a fine tuning varactor, and a negative resistance cell. Free running frequency is determined by the fixed capacitor and the inductor, and excessive frequency is controlled by the capacitance of the varactor. A small voltage fluctuation in one VCO output node is amplified by the back-to-back transistors. The amplitude of VCO is limited by the supply voltage, and the oscillation frequency is defined by the L and C values.

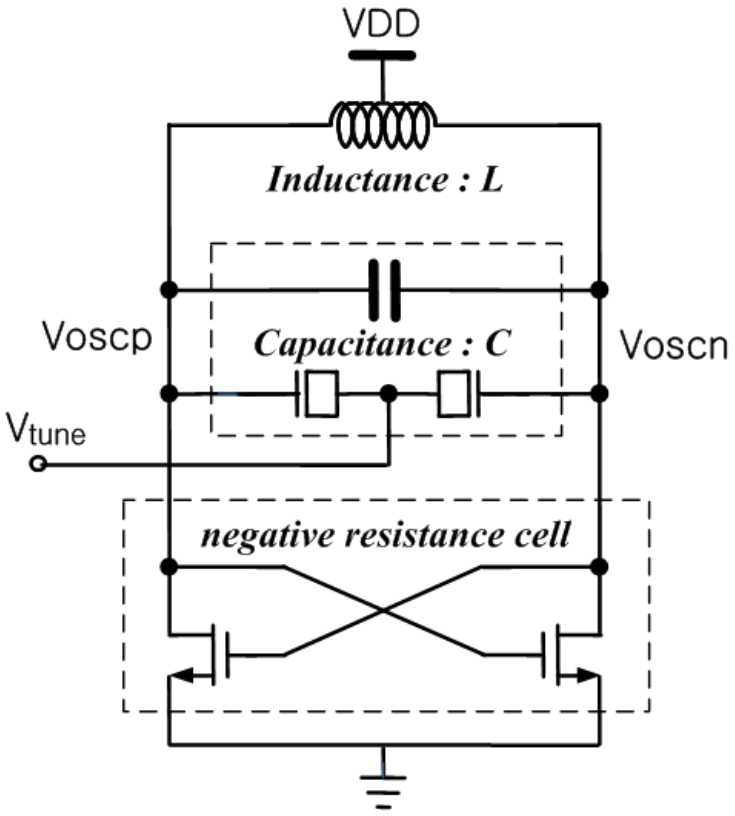


Figure 3.10. Typical LC-VCO.

Figure 3.11 shows a simplified negative resistance model of the LC-VCO for analysis [16]. The loss of the LC-tank due to parallel resistance is compensated by the negative resistance cell. The LC-tank energy is transferred from the capacitor to the inductor and vise versa. In the resonance condition, the oscillation frequency is given by

$$F_{vco} = \frac{1}{2\pi\sqrt{L \cdot C}} \quad \text{and} \quad R_p = -2/gm. \tag{11}$$

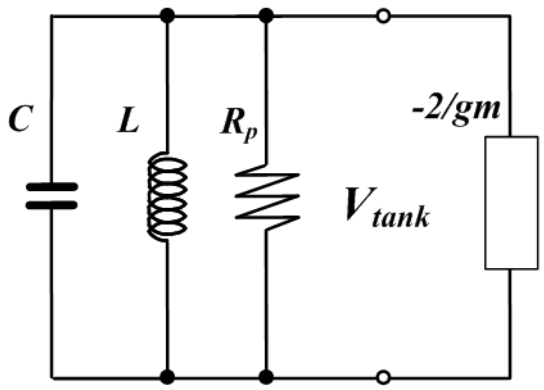


Figure 3.11. A simplified negative resistance model of a LC-VCO.

VCO phase noise is given by lesson's equation as follow [17].

$$L(f)=10\cdot\log\left[\frac{1}{2}\cdot\left\{\left(\frac{f_{vco}}{2\cdot Q_L\cdot f}\right)^2+1\right\}\cdot\left(\frac{f_{\frac{1}{f^3}}}{f}+1\right)\cdot\left(\frac{F\cdot k\cdot T}{P}\right)+\frac{2\cdot k\cdot T\cdot R\cdot {K_{vco}}^2}{f^2}\right] \quad (12)$$

F : $Noise\ Figure\ of\ active\ device$

k : $Boltzman's\ constant$

T : $Temperature$

P : $RF\ singal\ power$

Q_L: $loaded\ Q\ of\ inductor$

$f_{\frac{1}{f^3}}$: $\frac{1}{f}$ noise corner freqeuncy

R : $Noise\ resistance\ of\ varactor\ diode$

To reduce phase noise, large signal swing and high Q-factor are required.

3.3.2. Phase Frequency Detector

A PFD detects phase/frequency difference between two input signals and generates CP deriving signals proportional to the phase and frequency difference [18]. A tri-state PFD is shown in Figure 3.12(a). The PFD circuit includes two D-type flip-flops and an AND gate. The inputs of the flip-flops are tied to logic high. One flip-flop is clocked by the reference signal and the other is clocked by the feedback signal, divided down from the VCO output signal. The outputs of the flip-flops, U_p and D_n, are used to reset both flip-flops after the AND gate. The U_p and D_n signals are reset to logic low by a reset signal *Rst*. Since the PFD has three states, the case that both U_p and D_n are high does not exist. Figure 3.12(b) shows a state machine diagram of the PFD and Figure 3.13 illustrates a timing diagram of the operation of the PFD. The feedback signal usually has less than 10% duty cycle. However, since the PFD only detects the rising edge of the input signals, the duty cycle of the input signal is not important. The time difference between two rising edges of the input signals, $\Delta\tau$, is proportional to the phase difference between two inputs. The instantaneous phase difference can be expressed as

$$\Delta\phi = 2\pi \frac{\Delta\tau}{T}. \tag{13}$$

, where T is the period of the reference signal. Continual rising edges of the same signals cannot change the state but increase the phase difference. Therefore, even though the frequency difference between two inputs is large, the PFD drives right outputs, and the capture range is not limited. Figure 3.14 shows a normalized characteristic of an ideal tri-state PFD.

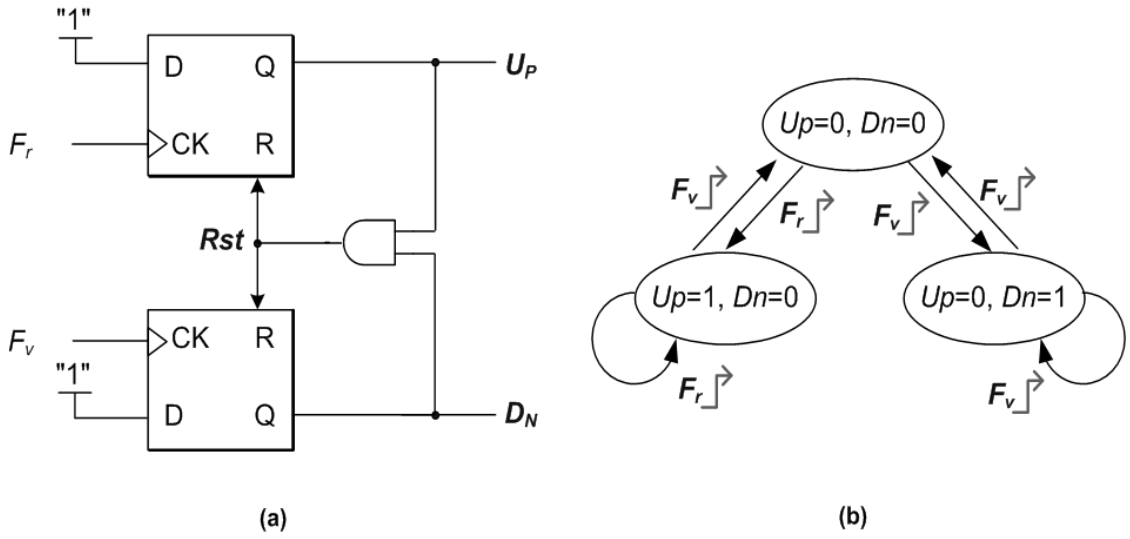


Figure 3.12. A block diagram (a) and a state machine diagram (b) of an ideal tri-state PFD.

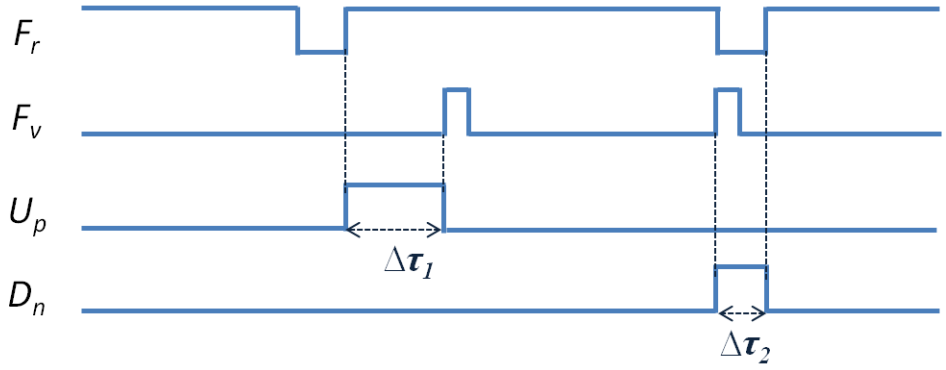


Figure 3.13. Timing diagram of an ideal tri-state PFD.

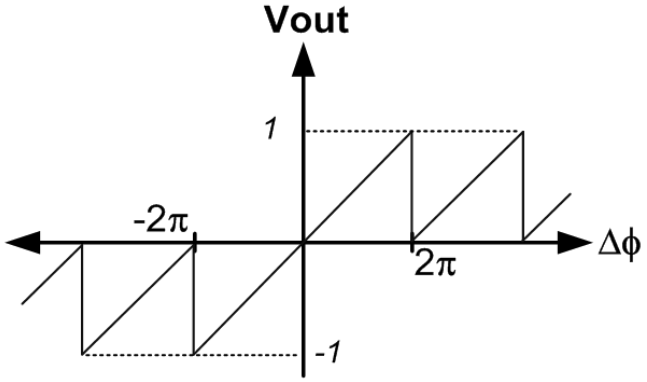


Figure 3.14. Characteristic of an ideal tri-state PFD.

Until now, the basic operation of an ideal PFD is considered. However, there are nonideal effects in real PFDs. When a PFD is combined with a CP, the PFD cannot drive the CP under locked condition because the phase difference between two input signals is so small. The CP does not response to the PFD outputs in this condition and dead zone takes a place around the zero crossing point in the characteristic curve.

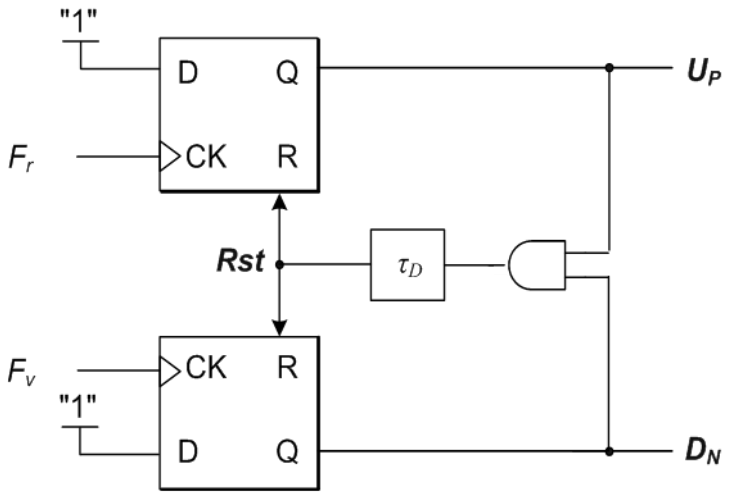


Figure 3.15. A block diagram of a tri-state PFD with a delay element.

Since the phase noise of the PLL output is seriously degraded with the dead zone, a delay element is added in the feedback path to guarantee enough turn-on time for the CP as shown in Figure 3.15. The U_p and D_n signals are simultaneously logic high for duration given by the delay element. The timing diagram shows this in Figure 3.16. The tri-state PFD with the delay element has fourth state, U_p and D_n are high, temporary whenever it is reset. The state machine diagram is modified from Figure 3.12(b) to Figure 3.17.

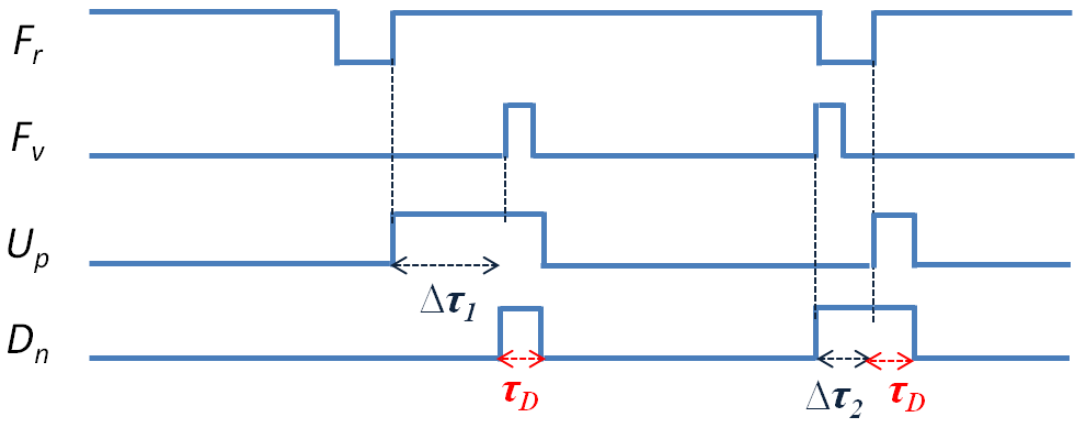


Figure 3.16. Timing diagram of a tri-state PFD with a delay element .

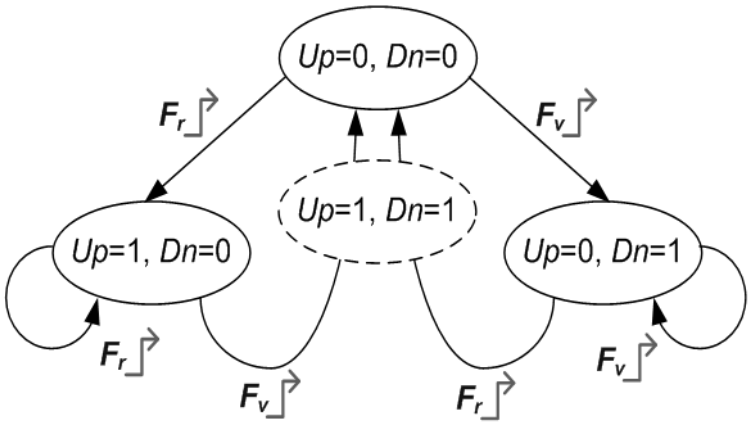


Figure 3.17. A state machine diagram of a tri-state PFD with a delay element.

3.3.3. Charge-Pump

A CP takes the U_p/D_n signals from the PFD and supplies charge to the LPF when the time period of U_p signal is longer than that of D_n signal. To the contrary, it sinks the charge stored in the LPF when the time period of U_p signal is shorter than that of D_n signal. Figure 3.18 shows a simplified CP circuit. Since the charging network consists of PMOSs and the sinking network consists of NMOSs, D_n and U_{pb} signals activate the CP.

When the U_{pb} turns on the charging path from the supply node to the CP output, the current I_{cp} is mirrored into the LPF. A cascode structure helps to reduce the channel length modulation effect and the I_{cp} is controlled by a fine current step to compensate the PLL-loop bandwidth variation [19].

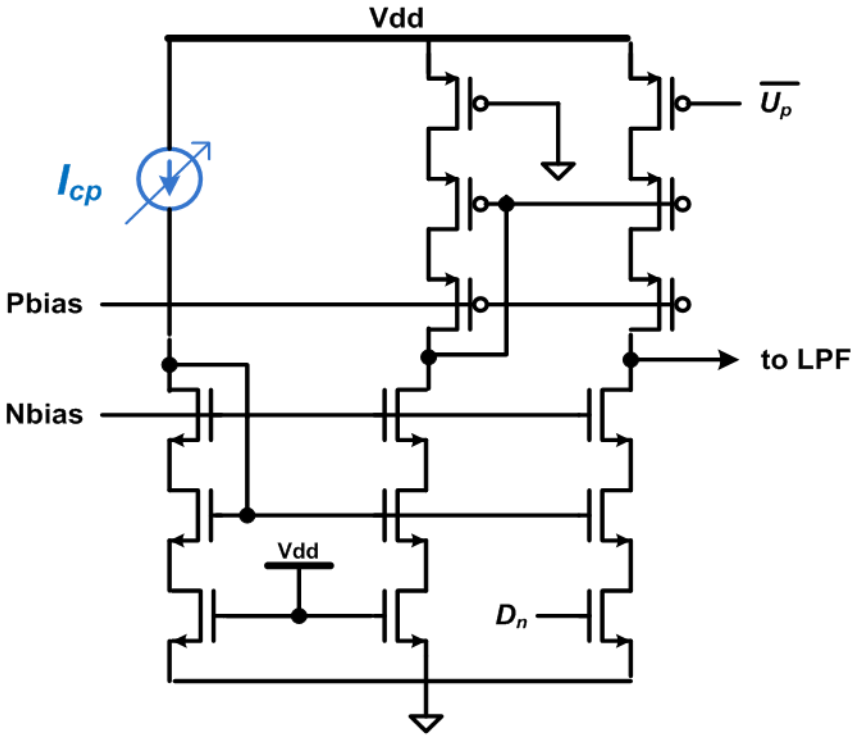


Figure 3.18. A simplified CP circuit.

The performance of the CP is evaluated together with the PFD, so the simulation should be done in conjunction with the PFD. There are several design considerations in the CP design. In this chapter, we check the effect of up/down current mismatch, up/down signal timing mismatch, voltage compliance, and noise floor. The noise floor determines the in-band phase noise contribution of the PFD/CP in the PLLs. The others degrade the performance of spurious tones.

A. Up / down Static Current Mismatch

Static up/down current mismatch results in an offset current in the CP output as shown in Figure 3.19. The example shows that the up current is higher than the down current by 10%. Since the PLL will balance total up/down current at locked state, the longer D_n signal is generated. Accordingly, the VCO tuning node fluctuates depending on the amount of current mismatch. To reduce the effect of up/down current mismatch on the VCO tuning node, the CP current should be increased or the dead-zone compensating delay should be lessened.

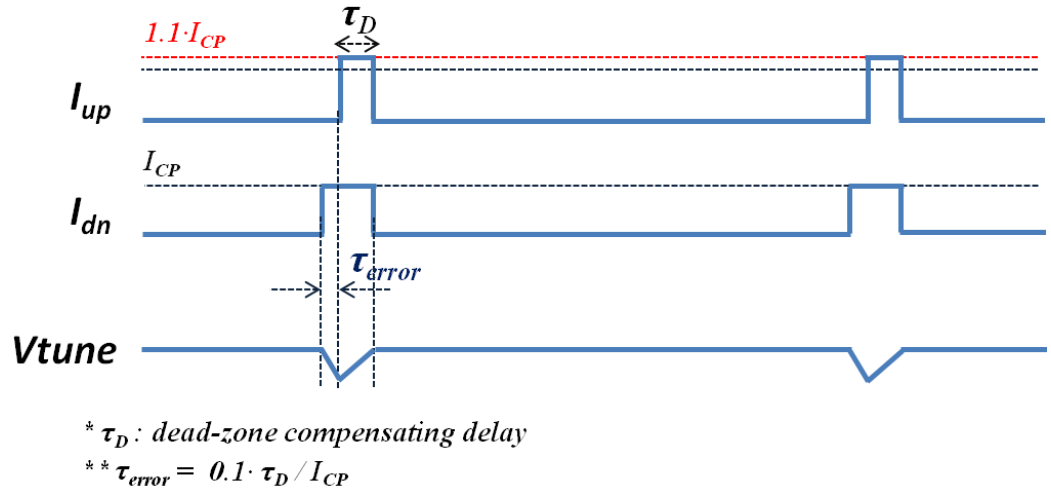


Figure 3.19. The effect of up/down current mismatch on *Vtune* in a CPPLL.

B. Up / down Signal Timing Mismatch

The mismatch of the path delay from the PFD to the CP for each U_p/D_n signal also causes the VCO tuning node to fluctuate. Since the U_{pb} signal path has more delay than

the D_n signal path, a transmission gate is used as a delay buffer as shown in Figure 3.20. The timing diagram to see the effect of this delay mismatch is shown in the Figure 3.21.

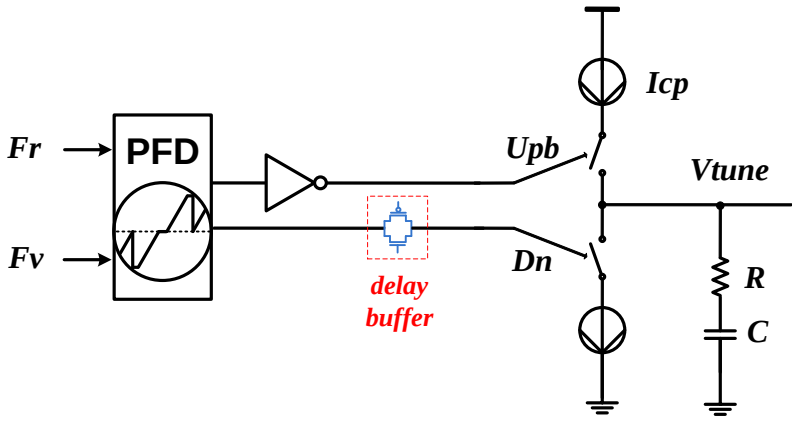


Figure 3.20. Delay buffer for Dn signal to reduce Up/Dn signal timing mismatch in a CPPLL.

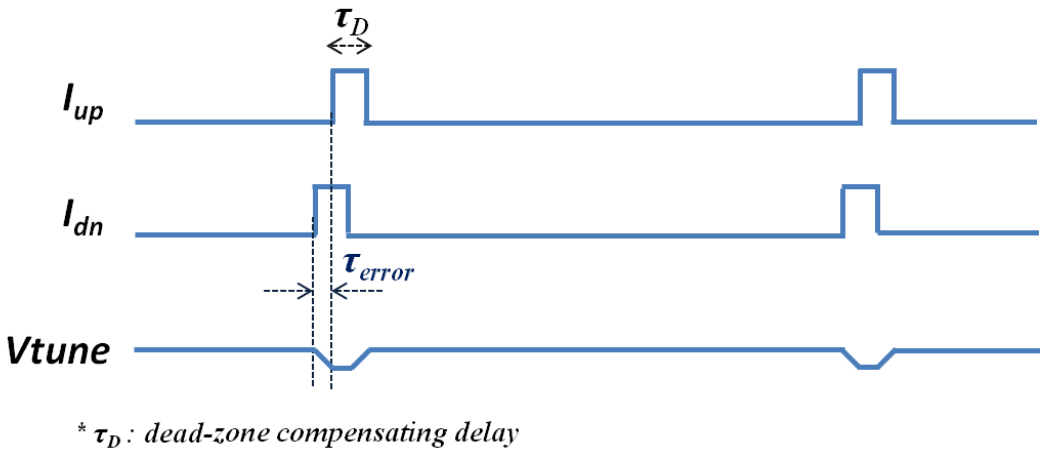


Figure 3.21. The effect of up/down current path delay mismatch on *Vtune* in a CPPLL.

C. Voltage Compliance

Since the CP output branch is a cascode type current mirror as shown in Figure 3.18, the DC output voltage affects the output current. Channel length modulation effect will

reduce the charging or sinking current with a DC voltage of around vdd/2. But, too much high or low DC voltage will crush the mirror circuit operation [20]. High output DC voltage increases sinking current but decreases charging current, thus the CP static U_p/D_n current mismatch increases. The CP output voltage should be confined within the voltage compliance range for high performance. Figure 3.22 shows sourcing and sinking current of a CP depending on DC output voltage.

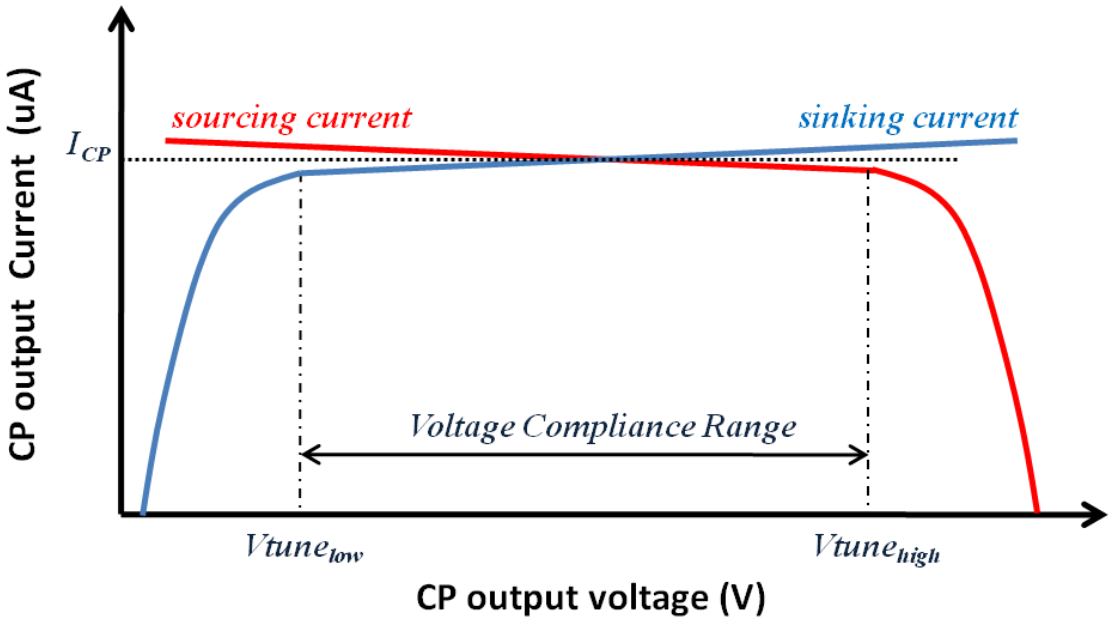


Figure 3.22. Voltage compliance range of a CP.

D. Noise Floor

The active devices in the CP generate channel noise, and the noise from the current source is mirrored into the CP output during the CP is activated. If the noise from supply or ground planes is excluded in the design stage, the noise floor can be calculated

with the output noise current of the CP. Figure 3.23 is an analysis of noise contribution of each transistor in the CP. The cascode transistor's noise contribution to the output is very small compared to others [21] and the noise from reference current is mirrored to the output. This noise gives a low limit of in-band phase noise in PLLs.

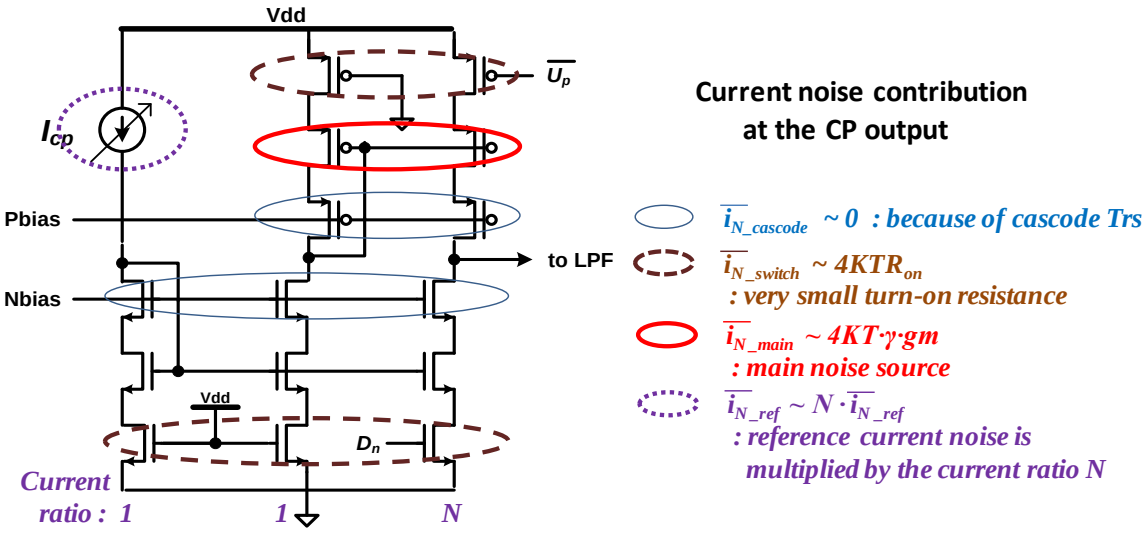


Figure 3.23. Current noise contribution at the CP output.

3.3.4. Loop Filter

A loop filter has two roles in the PLLs. It converters the CP output current to a voltage signal for VCO control. And it also smoothes out any out-of-band spurious tones. Even though large area is a disadvantage, second order or third order passive low pass filter is generally utilized since active filters add noise level. Figure 3.24 shows these two filter types.

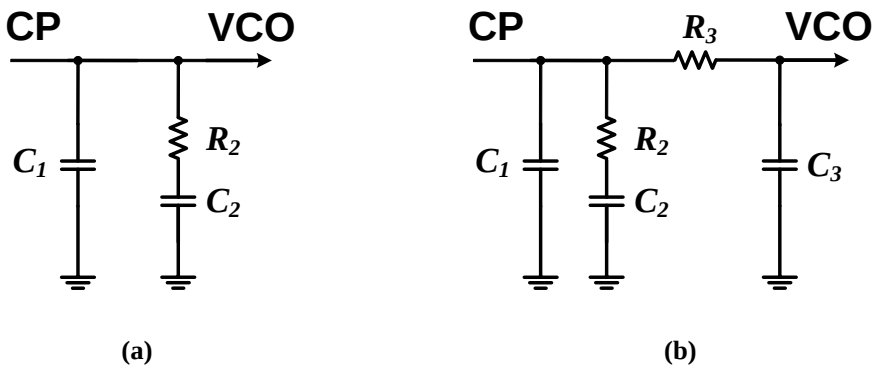


Figure 3.24. second order (a) and third order (b) loop filters in CPPLLs.

If we assume C_2 >> C_1 and C_2 >> C_3, the transfer function of each filter is expressed as follows.

$$H(s)=\left\{\frac{1}{sC_1}//\left(R_2+\frac{1}{sC_2}\right)\right\}\cdot\frac{\frac{1}{sC_3}}{R_3+\frac{1}{sC_3}}\approx\frac{1}{s(C_1+C_2)}\cdot\frac{1+\frac{s}{R_2C_2}}{\left(1+\frac{s}{R_2C_1}\right)\left(1+\frac{s}{R_3C_3}\right)} \quad (14)$$

From equation (14), poles and zero locations are found.

$$w_{p1}=0,\ w_{p2}=\frac{1}{R_2C_1},\ w_{p3}=\frac{1}{R_3C_3},\ w_z=\frac{1}{R_2C_2} \quad (15)$$

Since the loop filter has one pole and the VCO adds another pole at DC, CPPLLs have two poles at origin and the phase of an open loop PLL reaches -180 degree before the zero frequency. Therefore, phase margin is given by

$$\phi_{PM}=\arctan\left(\frac{w_{bw}}{w_z}\right)-\arctan\left(\frac{w_{bw}}{w_{p2}}\right) \quad (16)$$

, where w_{bw} is the loop bandwidth of the PLL. The bandwidth is calculated from the derivative of the equation (16). The derivative is

$$\frac{d\phi}{dw} = \frac{\frac{1}{w_z}}{1+\left(\frac{w}{w_z}\right)^2} - \frac{\frac{1}{w_{p2}}}{1+\left(\frac{w}{w_{p2}}\right)^2}. \tag{17}$$

Since it will be zero at the loop bandwidth of the PLL, the PLL bandwidth is expressed by

$$w_{bw} = \sqrt{w_z \cdot w_{p2}}. \tag{18}$$

Figure 3.25 shows the transfer function of a loop filter and an open loop PLL [22].

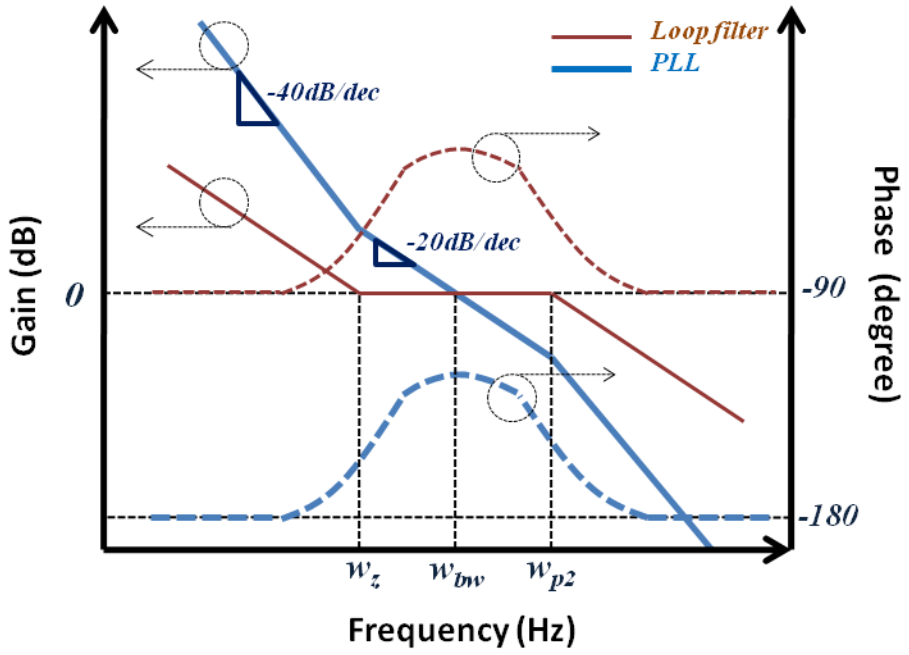


Figure 3.25. Transfer function of a loop filter and an open loop PLL.

3.3.5. Delta-Sigma Modulator

As a fractional engine, a DSM randomizes the output pattern to remove periodic tones. A basic DSM consists of an adder, an accumulator, and a quantizer as shown in Figure 3.26. The quantizer is modeled as an adder of an ideal signal and quantization noise for linear analysis. The quantization noise is modeled as additive white noise even though it is not uncorrelated with input signal [23]. Since the DSM operates on discrete-time base, the Z-domain transfer function is used. From the Figure 3.26, the signal and noise transfer functions are given by

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} = z^{-1},$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1},$$

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad , \tag{19}$$

, where *H(z)* is the transfer function of the accumulator. S_{TF} indicates that the input signal goes to the output with one clock time delay. However, N_{TF} shows that the quantization noise is shaped by a 1st-order high pass filter. Therefore, the quantization noise is suppressed in low frequency regime, providing high SNR. If we increase the order of the DSM, the higher SNR can be achieved. The benefits of DSM are randomization of the output bit pattern and noise shaping. Based on this characteristic, let's take look at the DSMs for FN-PLLs.

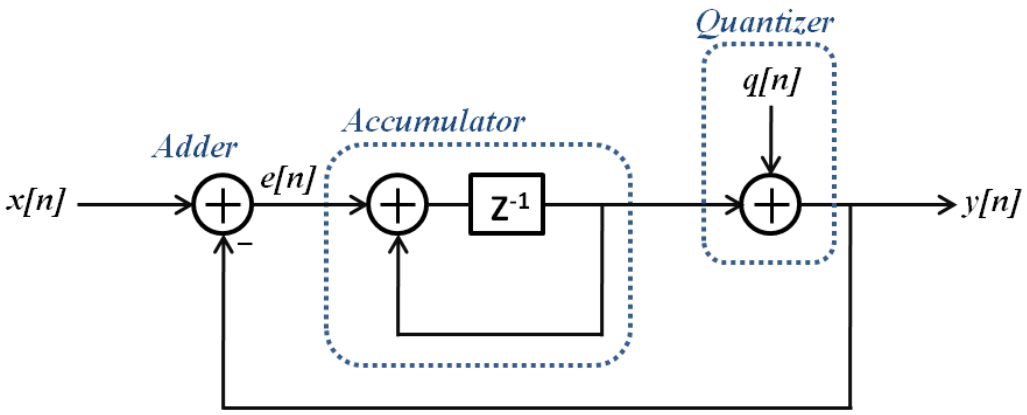


Figure 3.26. 1bit Delta-Sigma Modulator.

There are two different noise shaping architectures; interpolative type and *Multi-Stage Noise Shaping* (MASH) type. The MASH architecture is unconditionally stable, but its architecture is complicated, and each stage should have its own independent dither to provide the most uncorrelation of the quantization error and tends to generate wide-spread high-frequency hit patterns, resulting in more folding-in noise within the band [24]. An interpolative modulator is very simple and generates less high-frequency noise, but the full input range is not allowed because of its stability requirements. This limitation in the full input range causes the dead band problem that is a barrier to the single-bit interpolative architecture. In general, Butterworth filter coefficients are used to limit the pass-band gain level of the noise transfer function because of stability [25].

3.3.6. Prescaler and Divider

The programmable *N*-divider in the feedback path generates continuous integer division ratios without any discontinuity by using a pulse-swallow counter. Figure 3.27 shows a CPPLL with a typical pulse-swallow counter. It consists of a main counter, a

swallow counter, a dual modulus prescaler, and a control signal generator. Whenever the *MC* signal is activated, prescaler divides the VCO output by (P+1). If the total counting number is ***A*** and *MC* is activated during the counting number ***B***, the dividing value *N* is

$$N = \boldsymbol{B} \cdot (\mathrm{P}+1) + (\boldsymbol{A}-\boldsymbol{B}) \cdot \mathrm{P} = \boldsymbol{A} \cdot \mathrm{P} + \boldsymbol{B}. \qquad (19)$$

N can be any arbitrary integer values higher than P(P-1).

A divide-by-2/3 circuit is a basic cell in the prescaler. The P values can be increased by attaching divide-by-2 circuits at the end of the prescaler. For example, an 8/9 prescaler is implemented by attaching a divide-by-2 circuit to the 4/5 prescaler.

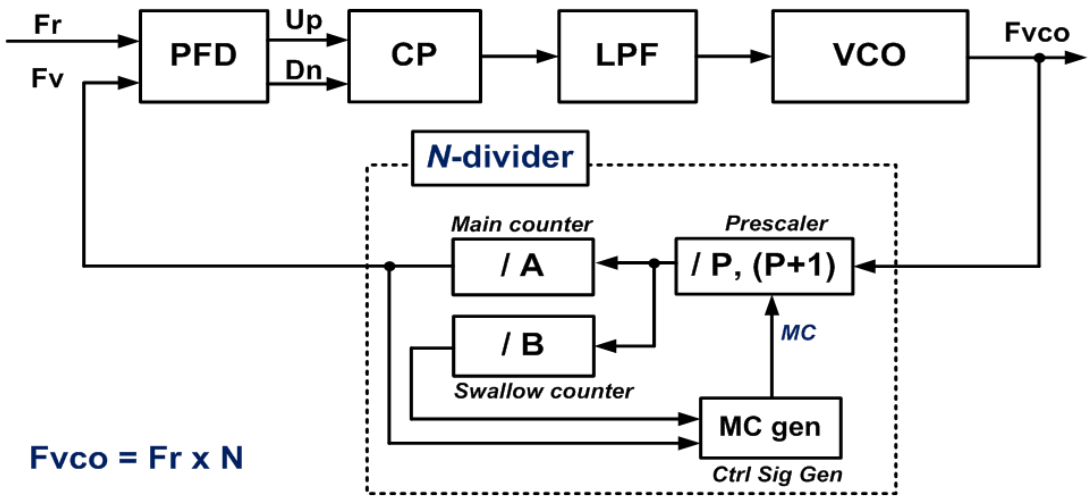
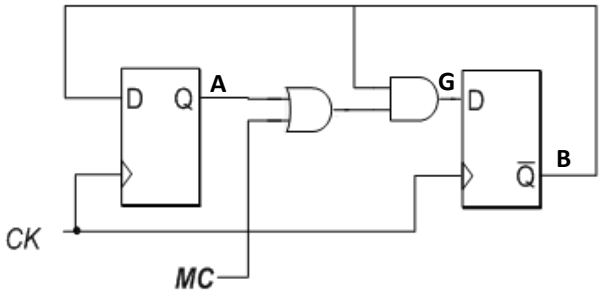


Figure 3.27. A CPPLL with a pulse-swallow counter.

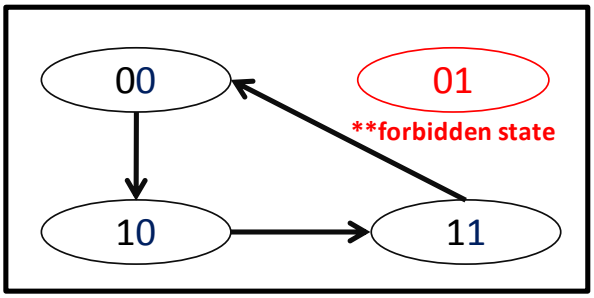
A divide-by-2/3 circuit and its operation are illustrated in Figure 3.28. When divide-by-3 circuit is enabled by the *MC* signal, one of four states is forbidden by the control signal as shown in the state machine diagram.



*When *MC* is low

Current State			Next State	
A	B	G	A	B
0	0	0	1	0
0	1	0	0	0
1	0	1	1	1
1	1	0	0	0

State machine diagram



Output sequence of B : 001001001001 …

Figure 3.28. Divide-by-2/3 circuit in a prescaler.

CHAPTER 4

CHALLENGES IN CHARGE-PUMP PHASE-LOCKED LOOP DESIGN

To design high performance CPPLLs for mobile communication systems, there are several design limitations to overcome. Some of them come from the stringent requirements for RF CPPLLs and others from the results of scaling down to deep submicron.

4.1. Limitation of Charge-Pump Phase-Locked Loop

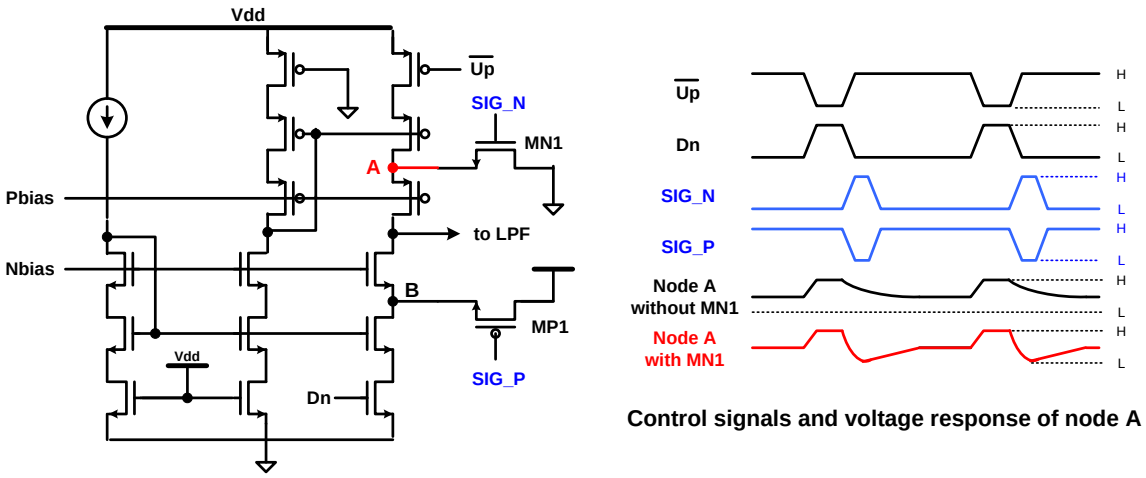
In this chapter, the limitations of RF CPPLLs and the solutions proposed already will be discussed. The last two parts are the motivation of this thesis. Even though many new ideas and solutions are proposed, there are too much room for improvement for the inherent drawback of CPPLLs, which is the U_p/D_n pulse train deteriorating the spectral purity in the PLL output.

At the moment, the scaling down to deep submicron is a main tendency in wireless transceiver design. But the supply voltage scaling limits the dynamic range of the analog circuits and it results in big performance degradation. For the CPPLLs, there are two issues; frequency range reduction and phase noise performance degradation. More detail explanation will be followed. To overcome these problems new proposals are presented in Chapter 5 and Chapter 6.

4.1.1. Nonlinearity of PFD/CP

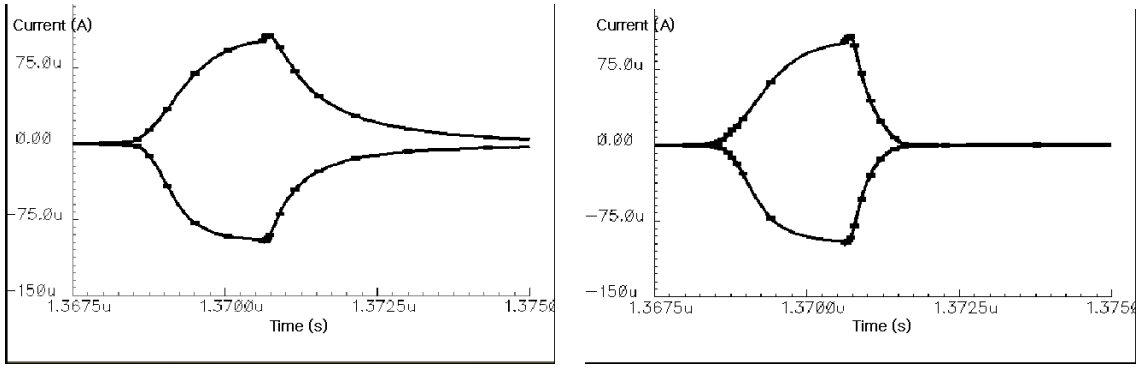
The first limitation of CPPLLs is the nonlinearity of the PFD/CP. Since the output of the DSM goes into the PFD/CP, digital data is converted to the analog domain. Even though the DSM has high SNR within in-band because of noise shaping characteristic, the nonlinearity in the PFD/CP results in noise folding. High level out-of-band noise is folded down to the in-band depending on the linearity. To increase the linearity, a static leaking current is intentionally included in the CP output. This changes the operating point of the PFD into U_p or D_n side instead of zero-crossing point, but increases reference spur level. Another way to improve the linearity is to reduce the CP turn-on or turn-off time [26]. By adding additional discharging path to the internal nodes of the CP, the turn-off time can be reduced as shown Figure in 4.1(a) [8].

When the U_p/D_n signals are turned off, conventional source-switching type CP is not turned off abruptly because the left drain charge of switching transistor loses discharging path and extends the turn-off time. To shorten the turn-off time, a CP with pull-up and pull-down transistors is introduced. The fast switching CP offers discharging paths when *SIG_N* or *SIG_P* signals are activated. As the activated time durations of *SIG_N* and *SIG_P* are very narrow compared with the period of reference clock, the charge of node A is restored before U_p/D_n signals are re-activated in locked condition. Timing diagram of node A without pull-down transistor, *MN1*, shows that the remained charge causes to increase the turn-off time (Figure 4.1b)). Figure 4.2 illustrates simulated on/off characteristics of with and without the pull-up/-down transistors. The faster CP shows faster switching property than conventional one.



(a) **(b)**

Figure 4.1. CP with pull-up and pull-down transistors (a) and timing diagram of node A (b).



(a) **(b)**

Figure 4.2. On/off characteristics of conventional source switching type CP (a), and fast switching CP (b).

4.1.2. Bulky Loop Filter

Large area of the LPF is the main limitation of CPPLLs. Since the noise from the LPF directly affects the VCO performance, passive bulky LPFs are used in the RF CPPLLs. As the technology scales down, the integration of LPF becomes more and more difficult. Even if capacitor multipliers, active filters, and digital domain solutions are

proposed, there are some issues such as active components' noise and efforts converting stabilized analog blocks to digital ones [27]. The stacked structure LPFs can save much area without serious performance degradation [8].

Figure 4.3 shows a third order stacked-structure LPF for CPPLLs. Each C1 and C2 has a stacked structure consisting of two *Metal-Insulator-Metal* (MIM) capacitors and a MOS capacitor. This architecture allows us to utilize limited area more effectively. With this stacked capacitor, the LPF area can be reduced to 40% of MIM only LPF. General concerns about MOS capacitors are capacitance variations depending on control voltage, process, and temperature variations, and leakage current. The simulated results of MIM and MOS capacitors depending on each condition is listed in Table 4.1.

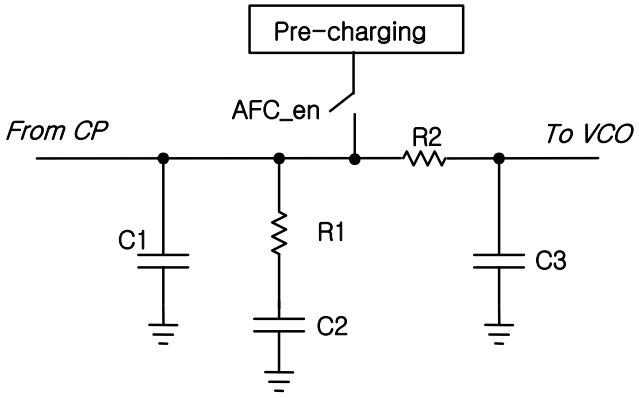
Table 4.1. Simulation results of MIM and MOS capacitors.

	SIMULATION CONDITIONS					
	NNNNN **100**	NNNNN **27**	NNNNN **-30**	**FFFFF** 27	**NNNNN** 27	**SSSSS-** 27
CMOS (△Cmos)	278.8 pF (-0.34%)	279.8 pF (0%)	281.1 pF (0.46%)	286.5 pF (2.4%)	279.8 pF (0%)	278.8 pF (-2.29%)
Cmim (△Cmim)	202.8 pF (0%)	202.8 pF (0%)	202.8 pF (0%)	182.8 pF (-10%)	202.8 pF (0%)	223 pF (9.96%)
	WORST-CASE SIMULATION CONDITIONS					
	SSFFF, 100, Vtune = 1.0		NNNNN, 27, Vtune = 1.2		FFSSS, -30, Vtune = 1.4	
Ctot (△Ctot)	445.9 pF **(-7.6%)**		482.6 pF **(0%)**		514.1 pF **(6.53%)**	

* Ctot = Cmos + Cmim

One thing to consider in the case of the MOS capacitor is the VCO tuning voltage. In this case, the targeting voltage tuning range is form 1.0V to 1.4V, but the range from 0.8V to 1.6V is set in simulation. This narrow tuning range is obtained from the excess 8-bit *Automatic Frequency Calibration* (AFC). The number of AFC bit is intentionally increased. As a result, the final capacitance variation range in stacked capacitor is from –

7.7% to 6.53%, whereas MIM only capacitor is from –10% to 9.96%. The leakage level is not so critical to degrade the reference spur characteristic. Capacitance variation of 8% can degrade phase margin of less than 2 degree or so in PLL. Pre-charging block is activated at the beginning of AFC mode and charges the LPF to vdd/2 to reduce PLL settling time in closed loop condition.



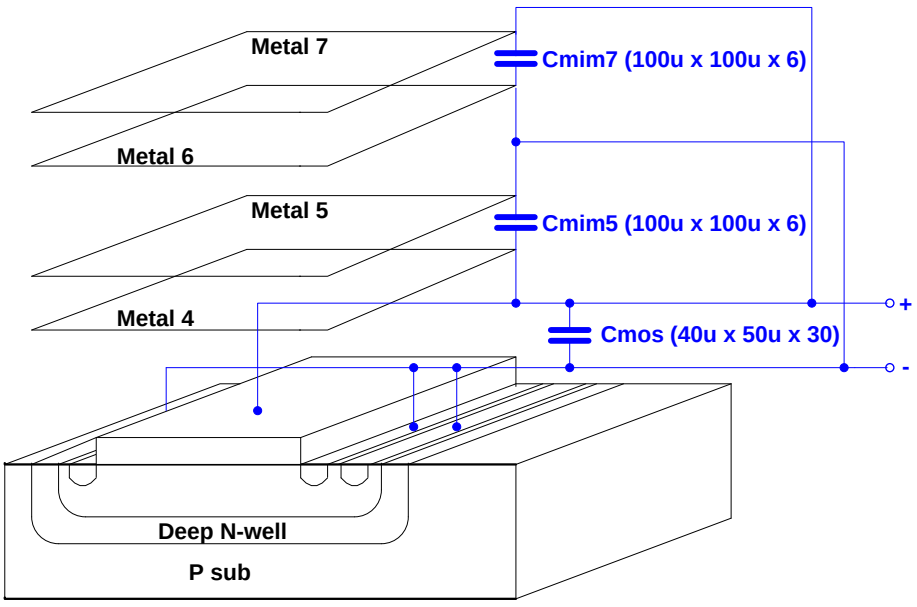


Figure 4.3. Structure of a stacked capacitor.

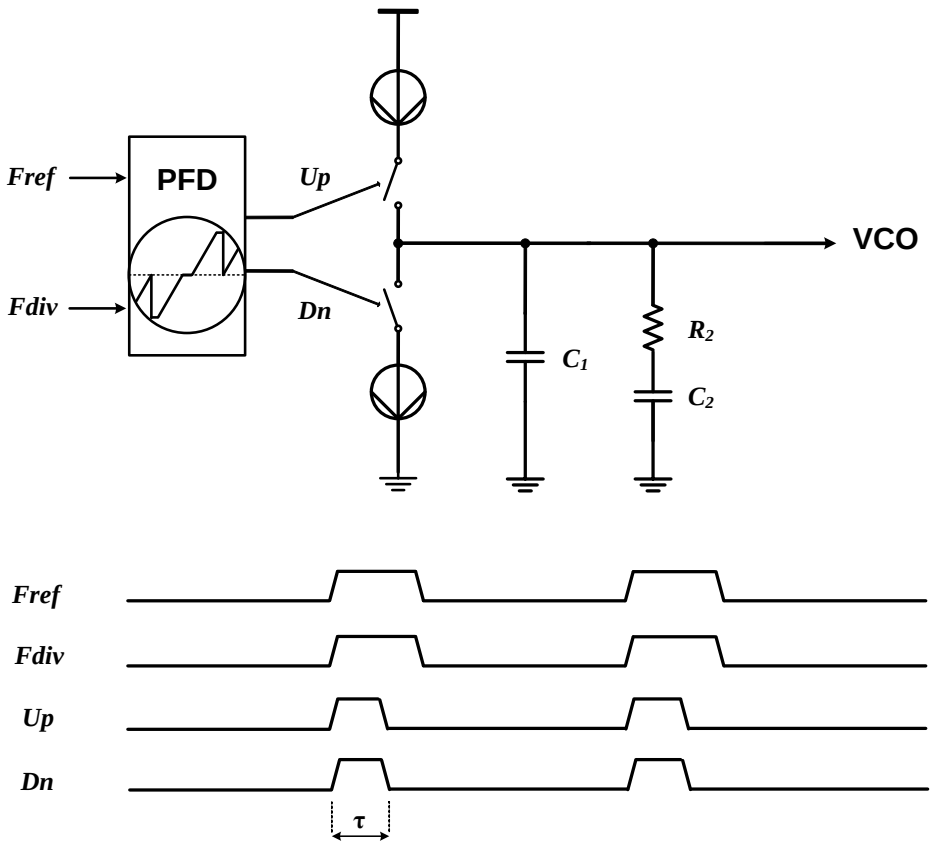


Figure 4.4. A charge-pump PLL and its periodic pulses, disturbing the VCO tuning node, under the locked condition.

4.1.3 Continuous U_p/D_n Current Pulses

CPPLLs produce periodic pulses in the CP outputs and generate ripples on VCO tuning nodes in accordance with a reference clock. The VCO tuning nodes are very sensitive to any disturbance such that 2nd- or third order passive LPFs with a large area are

required to smooth out the ripples. The passive LPFs cannot eliminate but only suppress them depending on offset frequencies. Thus, these pulses are the sources of reference

spurs and degrade the phase noise of the CPPLLs disturbing VCOs. Also, the noise coming from supply and ground planes degrades phase noise performance, along with the thermal and flicker noise of the CP transistors, while the CPs are activated by the signals from PFDs. Even though the CPPLLs are in locked state, the periodic pulses are generated because the PFDs include delay cells to prevent 'dead-zone problem'[28]. Figure 4.4 illustrates this, where F_{ref} and F_{div} are reference and feedback signals, respectively. U_p and D_n represent PFD outputs. Therefore, the U_p and D_n signals are activated simultaneously during every reset period, and phase noise degradation as well as reference spurs is unavoidable in the CPPLLs.

4.2. Design Challenges Due to Scaling down to Deep Submicron

Even thought the scaling down to deep-submicron CMOS technologies gives some benefits such as high integration capability, faster transistor, better geometrical matching, and low power consumption, the dynamic range reduction with lower supply voltages is a stringent design challenge [29]. The reduced available voltage swing limits compliance voltage, the maximum voltage of a current source operating properly, of CPPLLs and tuning voltage range. The total frequency range of a VCO is give by

$$F_{range} = K_{vco} * \triangle Vtune \tag{20}$$

, where K_{vco} and $\triangle Vtune$ are VCO gain and tuning voltage range, respectively. Therefore, the total frequency range of the VCO is reduced. Also, phase noise of the VCO is express as

$$PN = 10\,log\left(\frac{\overline{v_n^2}}{v_{sig}^2}\right) \tag{21}$$

, where $\overline{v_n^2}$ is squared noise voltage and $\overline{v_{sig}^2}$ is squared carrier voltage. This equation implies that the smaller signal swing in the VCO core degrades phase noise.

CHAPTER 5

THIRD ORDER SAMPLE-HOLD LOOP FILTER DESIGN

5.1. Introduction

Since PLLs generate carriers for transmission and LO signals for reception in RF transceivers, RF signals are directly affected by them and the spectral purity of the PLLs is critical to the overall system performance. A CPPLL has become the most general solution for frequency synthesis because it has an infinite gain for a static phase difference and capture range is not limited if the tuning node of a VCO is within voltage compliance range [11]. However, as mentioned in Chapter 4, the continual pulse train in the output of the CP seriously degrades the spectral purity in the CPPLLs.

To avoid this problem, digital-intensive approach such as an *All Digital PLL* (ADPLL) is introduced. ADPLLs have the advantage of a higher level of integration [30]. Since, except the *Digitally Controlled Oscillator* (DCO), whole blocks are digital circuits designed and synthesized using the *Hardware Description Language* (HDL), pre-designed blocks can be easily reused for new advanced technologies. Moreover, periodic pulse trains do not exist in the ADPLLs and the LPF is realized in digital domain with a small area. Nevertheless, the ADPLLs have limitations originated from the nature of digital circuits such as finite resolution and enormous switching noise. The entire blocks operate rail-to-rail according to the reference clocks at the same time, generating a lot of tones.

One of the simplest ways to improve the phase noise and spurious tone performance of the CPPLLs is to disconnect the signal path from the CP output and protect the VCO tuning node when the CP is activated. It is reported that loop filters incorporating sample-and-hold circuits improve phase noise and reduce reference spur levels [31]-[33]. Generally, a simple sampler, consisting of a MOS switch and a capacitor, is used to reduce additional hardware complexity. However, performance improvement is limited by the MOS switch due to its non-ideality.

In this Chapter, a third order switched sample-hold loop filter is presented for high spectral purity in a CPPLL [34]. The proposed LPF includes two MOS switches for phase noise improvement and spur level reduction. Each switch enhances in-band and out-of-band phase noise performance, respectively. The charge injection and clock feed-through from the MOS switches are minimized by controlling the size of the MOS devices and the switching time.

5.2. Prior Arts

5.2.1 Loop Filter with a Sample-and-Hold

To improve the spectral purity of the PLL output, a sample-and-hold is merged to the LPF to shield the VCO tuning node. A loop filter with a sample-and-hold circuit and simulation results in time domain with and without the sample-and-hold circuit are shown in Figure 5.1. The active sample-and-hold circuit is inserted into between the CP out and LPF. The simulation results in time domain shows the big improvement in spurious tone

performance. However, these active components generate additional noise at the VCO tuning node and hardware complexity also increases. To simplify the sample-and-hold circuit, sample-hold loop filters are proposed.

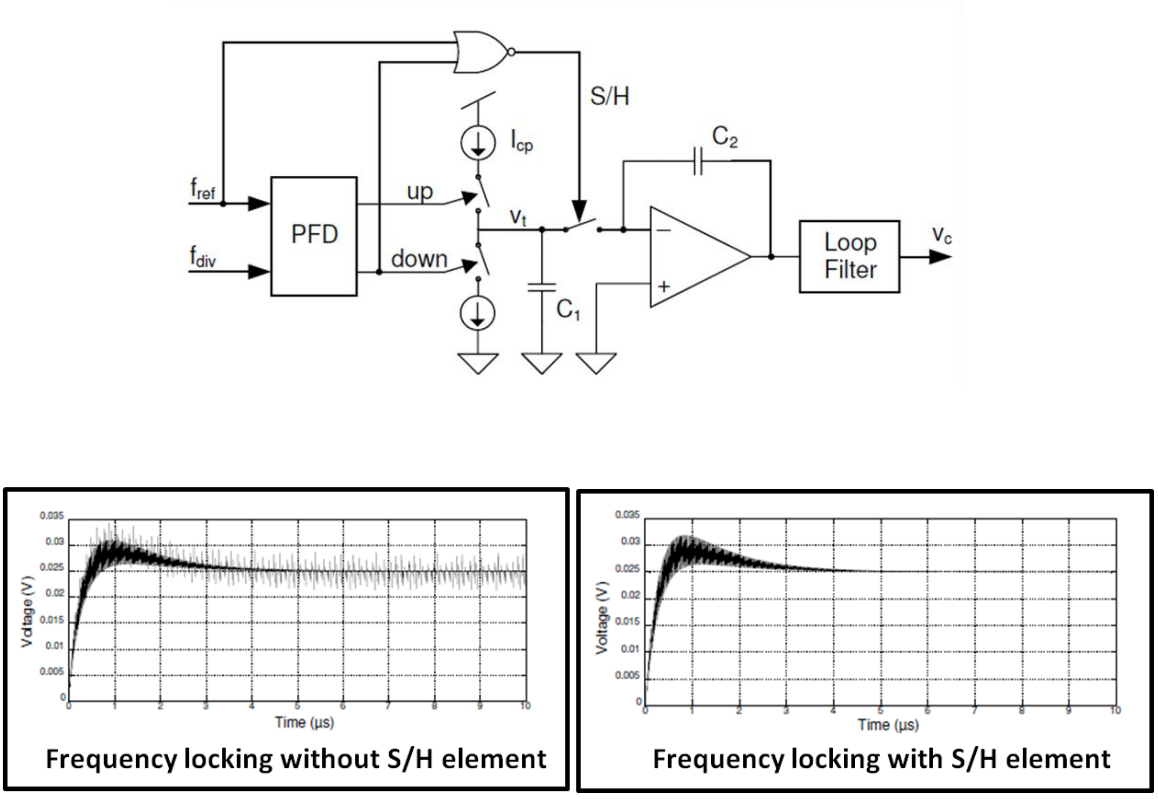


Figure 5.1. Loop filter with a sample-and-hold circuit, and simulation results in time domain with and without the sample-and-hold circuit.

5.2.2 Second Order Sample-Hold Loop Filter

A typical second order loop filter for a CPPLL consists of two capacitors and one resistor, and the VCO tuning node is directly connected to the output of a CP. To realize a sampler, the second order sample-hold loop filter includes a MOS switch, *sw*, and an additional capacitor, C_{1B}, as shown in Figure 5.2, where *Vsw* is the control signal of the

MOS switch [33]. Figure 5.3 shows the timing diagram of the control signals. The MOS switch disconnects the signal path when the current from/to the loop filter is triggered. The CP charges or discharges capacitor, C_{1A}, according to the PFD output, but the VCO tuning voltage remains the same during disconnection. After both NMOS and PMOS devices of the CP are turned off, the tuning node is reconnected and the tuning voltage is updated. If the switch is ideal and there is no settling process after reconnection, the reference spur will be eliminated and the phase noise degradation due to PFD/CP operation will not exist. However, the switches are implemented with MOS devices, thus, the non-ideal effects of the switches, such as turn-on resistance, charge injection, and clock feed-through, degrade the performance of the sample-hold loop filter [35].

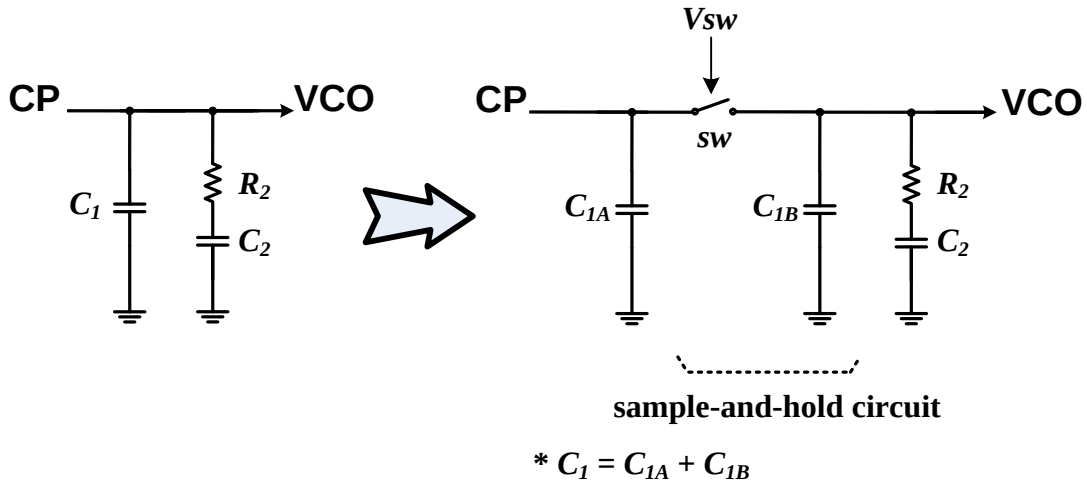


Figure 5.2. Conventional second order sample-hold loop filter.

Since the switch is in the middle of the signal path, the size should be as large as possible to minimize turn-on resistance because large turn-on resistance degrades or even changes the PLL loop dynamics. But large switches add more parasitic capacitance,

resulting in more charge injection and clock feed-through. Another drawback of the second order sample-hold loop filter is that the settling process of newly dumped charge starts as soon as the switch is closed because the main factors of the settling process, R_2 and C_2, are seen from the CP when the loop is connected. Some of newly dumped charge is transferred from C_{1A} to the VCO tuning node because of charge redistribution and the VCO tuning node experiences a settling disturbance.

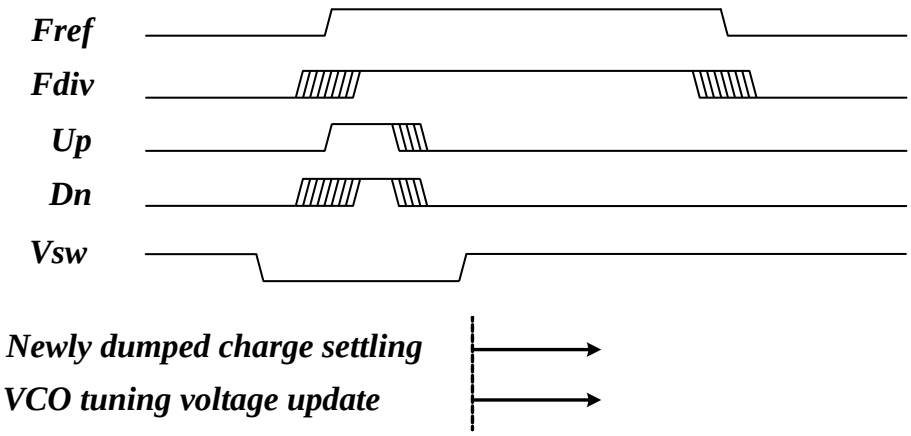


Figure 5.3. Timing diagram of the control signals in conventional second order sample-hold loop filter.

5.3. Third Order Sample-Hold Loop Filter with Two Switches

In order to improve the performance of the CPPLLs incorporating sample-hold loop filters, the effect of non-ideality in the MOS switches should be minimized. Since the channel charge is injected to the drain and source nodes of the switches when they are turned on or off, the charge injection effect increases with the device size. The clock feed-through effect due to the overlap and fringe capacitance of the MOS device also increases with the size. Therefore, minimum size switches are the best choice for the sample-hold loop filter.

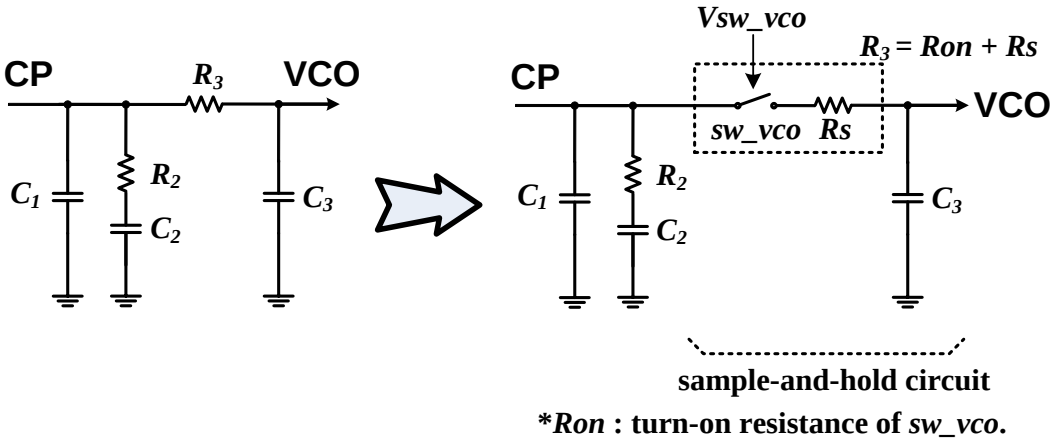


Figure 5.4. Proposed third order sample-hold loop filter with one MOS switches.

The first approach is to include a minimum size MOS switch to realize a sampler without degrading performance. A third order LPF can suppress more out-of-band noise than the second order LPF. Moreover, a series resistor exists in the signal path. Figure 5.4 shows a third order sample-hold loop filter with one MOS switch, *Vsw_vco*. Figure 5.5 illustrates the associated timing diagram. Since the turn-on resistance, R_{on}, as well as R_s is considered in the stage of loop filter design and the resistance of R_s is much larger than R_{on}, the size of MOS devices can be minimal. Therefore, charge injection and clock feed-through effects can be minimized.

The operation is as follows. When either U_p or D_n is activated, the VCO tuning node is separated from the CP output by *Vsw_vco*, and the charge stored in C_3 sustains the tuning voltage during disconnection. In contrast to the second order loop filter, even though the settling process has started because R_2 and C_2 are seen from the CP, the VCO tuning node is still disconnected by *Vsw_vco*. Reconnection is triggered by the falling edge of F_{ref}. The third order LPF settles down for a half period of the reference clock before reconnection, while the second order LPF starts a settling process after

reconnection. This modification reduces the fluctuation range of the VCO tuning node and improves the in-band phase noise of the CPPLL.

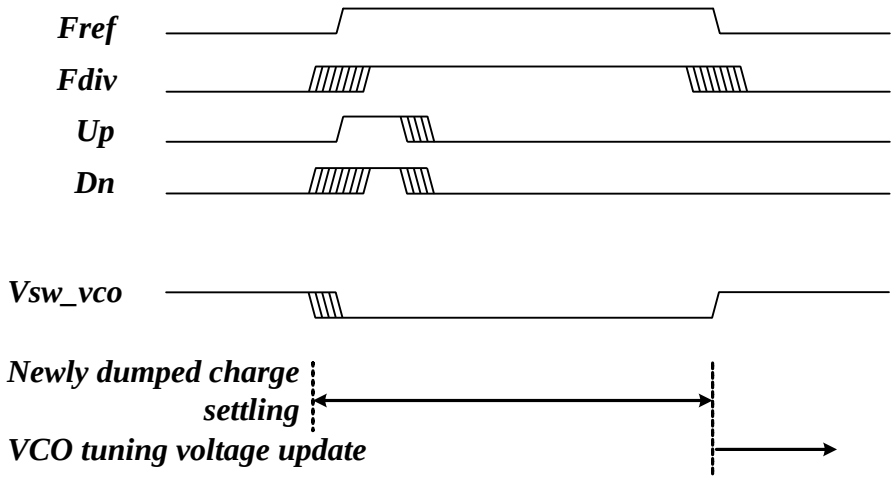


Figure 5.5. Timing diagram of the proposed third order sample-hold loop filter with one MOS switches.

To enhance the performance further, another switch, *sw_cp*, is added. Figure 5.6 shows the final third order sample-hold loop filter with two MOS switches and the associated timing diagram, where *Vsw_cp* and *Vsw_vco* are control signals for the *sw_cp* and *sw_vco*, respectively. The VCO tuning node is separated from the CP by both *Vsw_cp* and *Vsw_vco* when either U_p or D_n is activated. Once the PFD is reset, the switch *sw_cp* is turned on. At the same time, the settling process starts. Reconnection is triggered by the falling edge of *Fref* after a half period of the reference signal. The switch *sw_cp* disconnects the R_2 and C_2 from the CP whenever the charging or discharging path is activated. Since *sw_cp* is in the middle of the signal path, the size of the MOS devices is much larger than that of *sw_vco*. But, the charge injection and clock feed-through are not problematic because the VCO tuning node is still disconnected by *sw_vco* when

sw_cp is turned on. The benefit of *sw_cp* is that the CP switching noise and the induced noise from supply and ground planes are not directly coupled to the LPF when the CP is activated. High-frequency noise bypasses through C_1 and the out-of-band phase noise performance is improved.

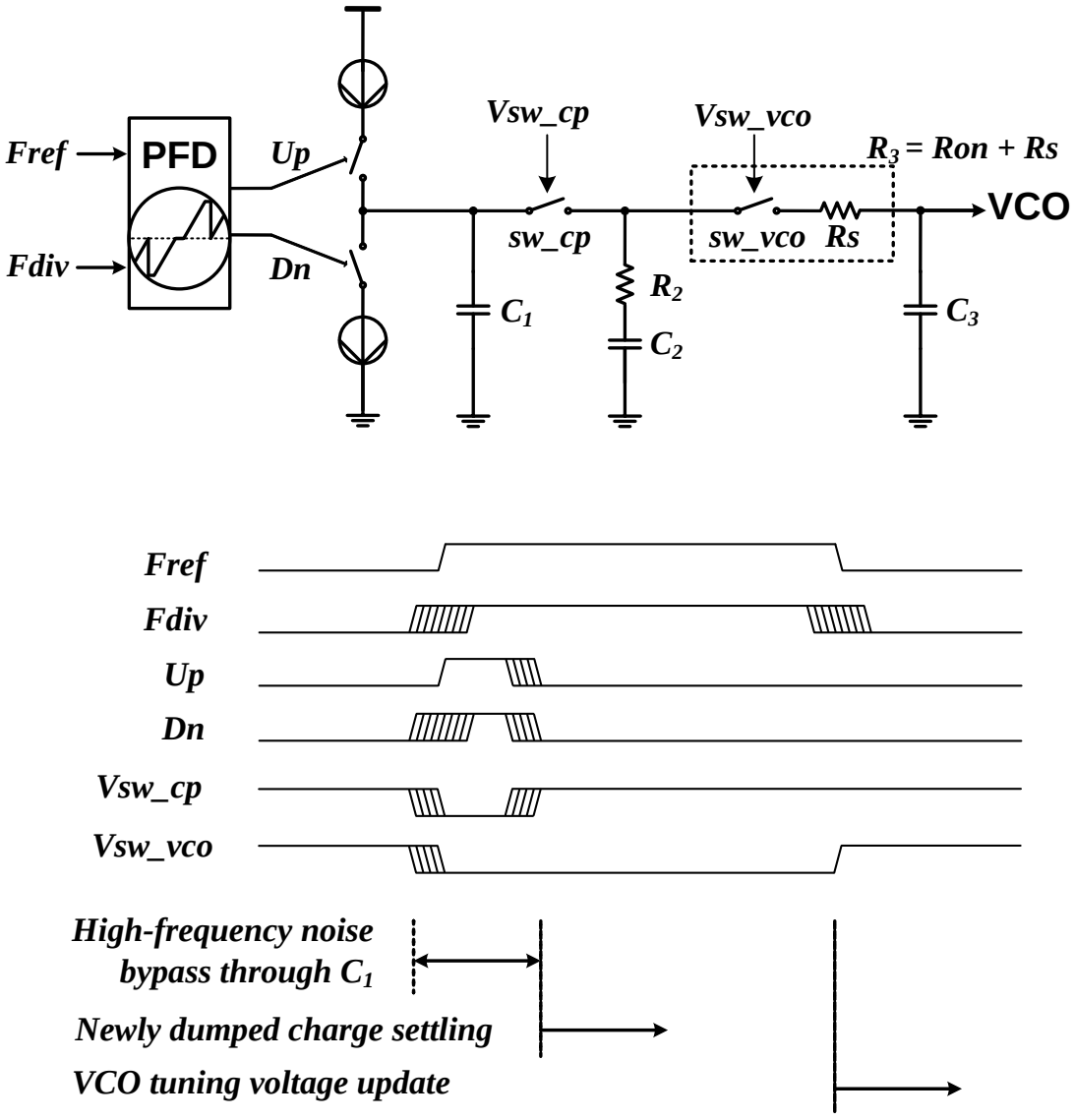


Figure 5.6. Circuit and timing diagram of the proposed third order sample-hold loop filter with two MOS switches.

5.4. Measurement Results

The proposed third order switched sample-hold LPF is designed and fabricated within a CPPLL using a 45-nm SOI-CMOS technology. The performance evaluation is done with a 26 MHz reference clock and a 1.248 GHz VCO output frequency. Figure 5.7 shows the measured phase noise of the CPPLL. When both *sw_cp* and *sw_vco* are deactivated, it simulates a conventional LPF without a sample-hold element. The in-band phase noise is -70 dBc/Hz, and the out-of-band phase noise shows -101 dBc/Hz at 400 KHz offset frequency. To simulate the second order sample-hold loop filter, only *sw_cp* is activated. In this case, the out-of-band phase noise has been improved up to 9 dBc/Hz at the offset frequency from 100 KHz to 1 MHz, maintaining a similar in-band phase noise level.

Only *sw_vco* is activated for the case of the proposed LPF with one MOS switch, and the in-band phase noise is improved up to 8 dBc/Hz with the same out-of-band phase noise level as in the first case. Therefore, the phase noise of both in-band and out-band can be improved when the two switches are activated at the same time. As a result, the proposed loop filter provides up to 8 dBc/Hz phase noise improvement in in-band and 9 dBc/Hz in out-of-band, compared with the conventional case.

Figure 5.8 shows the measured reference spurs. The SOI process provides good isolation and small parasitic capacitance due to higher resistance of the substrate and a buried oxide layer. Therefore, the conventional LPF exhibits a low spur level. However, the proposed filter reduces the spur level by 7.25 dB and enhances the tone performance further. The performance improvement by the proposed LPF is summarized in Table 5.1.

The chip photo of the proposed sample-and-hold loop filter is in Figure 5.9. The active area including PLL core and test block is 0.138 mm^2.

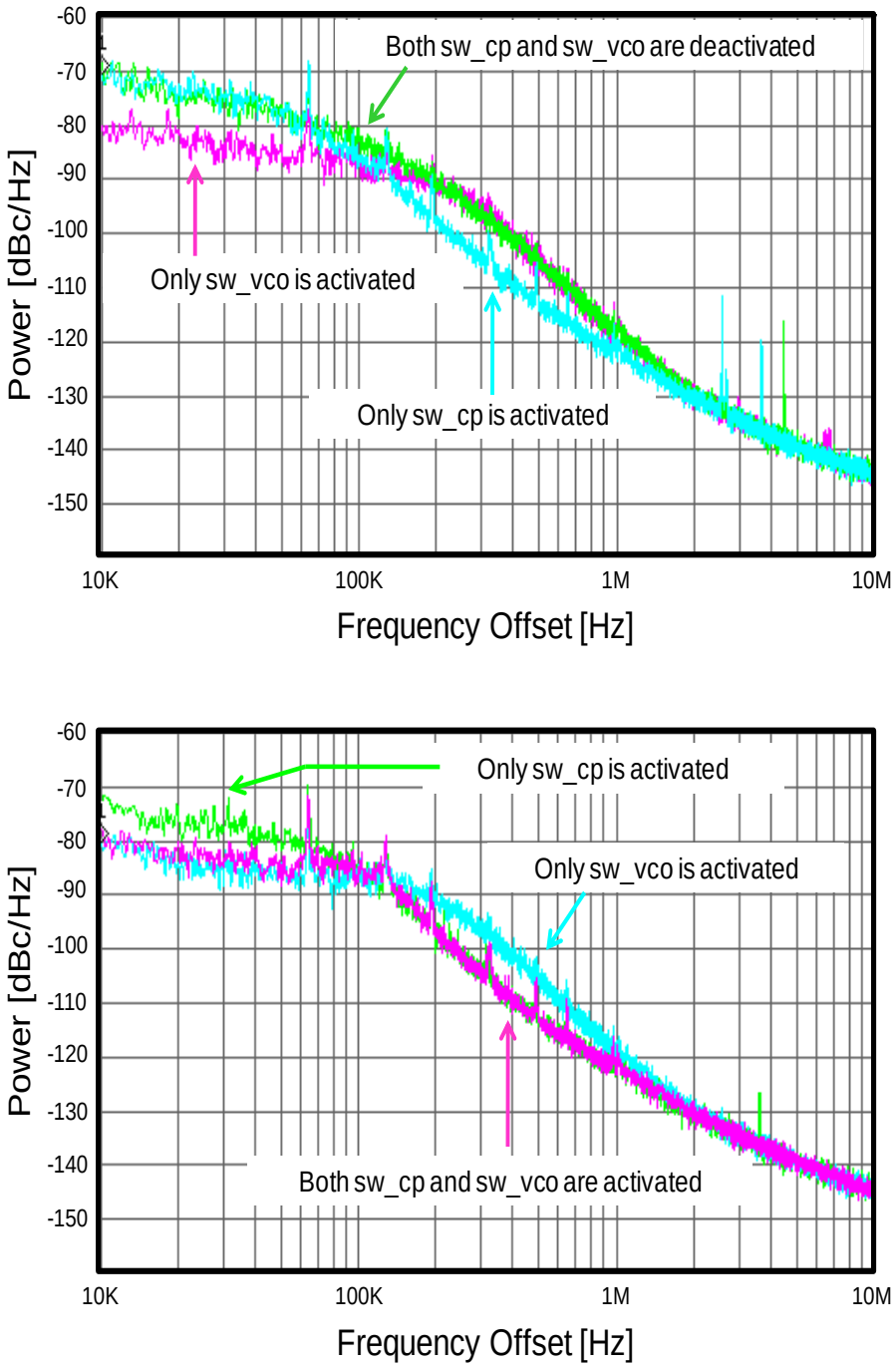


Figure 5.7. Phase noise improvement by the proposed loop filter. The sw_cp switch improves out-of-band phase noise, and the sw_vco switch improves in-band phase noise.

Table 5.1.
Performance improvement by the proposed 3rd–order sample-hold LPF.

In-band Phase Noise (Fout = 1.248 GHz)	8 dBc/Hz @ 20 KHz
Out-of-band Phase Noise (Fout = 1.248 GHz)	9 dBc/Hz @ 400 KHz 2 dBc/Hz @ 1 MHz
Reference Spur Level	7.25 dB

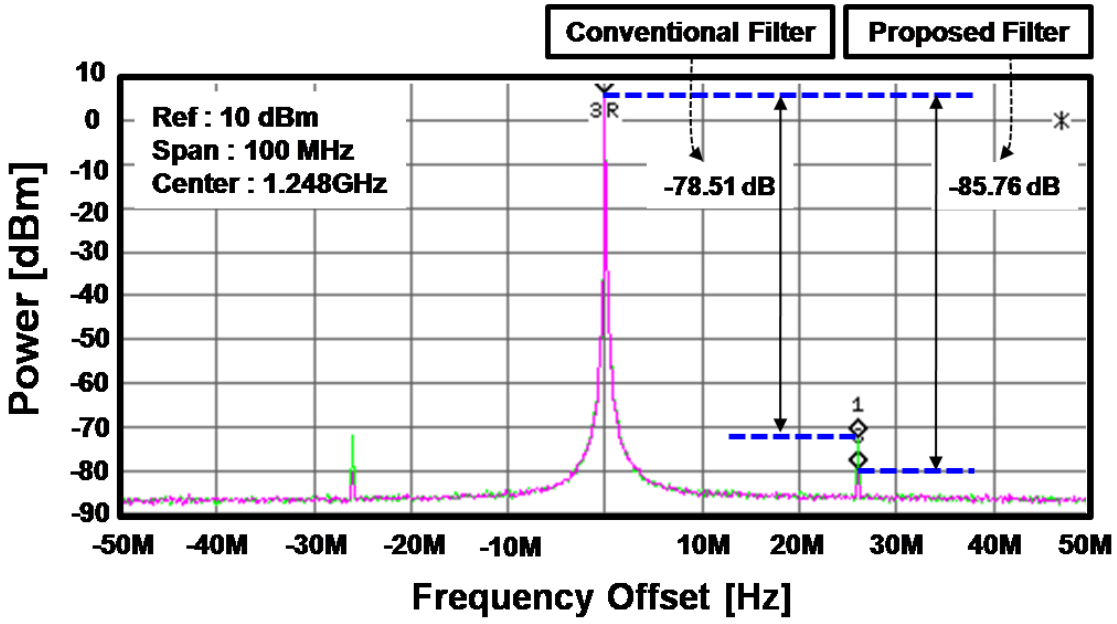


Figure 5.8. Measured reference spurs and the proposed loop filter reduces the spur level by 7.25 dB.

5.5. Conclusion

In this research, a new third order sample-hold loop filter in a RF CPPLL for high spectral purity is proposed. It disconnects the CP output during the CP activation period and shields the VCO tuning node from any disturbance. By adopting the third order filter architecture, the switch for the sample-and-hold can be designed with a minimum size, and this enables the nonideal effects of the MOS switches such as, clock feedthrough and

charge injection to be minimized. Two switches improve the in-band and out-of-band noise at the same time. Measured results show good phase noise and spurious tone performance in the proposed LPF compared with the conventional architecture. the proposed loop filter provides up to 8 dBc/Hz phase noise improvement in in-band and 9 dBc/Hz in out-of-band. The reference spur level also has been improved by 7.25 dB. The LPF was integrated within a full frequency synthesizer for mobile communication systems in a 45-nm deep sub-micron SOI-CMOS technology. Active area for the proposed LPF is 0.048mm^2.

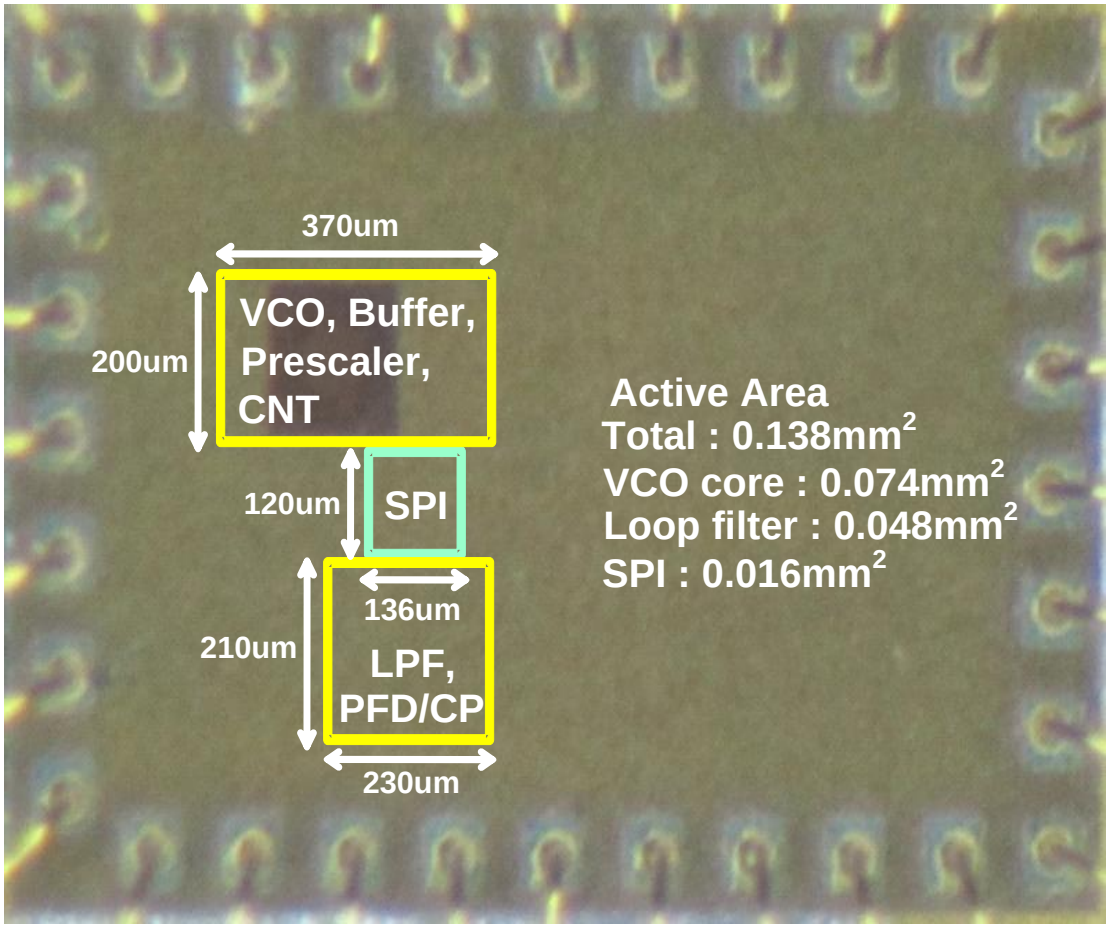


Figure 5.9. Chip photo of the proposed third order sample-hold loop filter.

CHAPTER 6

WIDEBAND PHASE-LOCKED LOOP DESIGN

6.1. Introduction

Wideband PLLs supporting multiple standards with a single VCO are very attractive because die area can be saved by circumventing multiple VCOs and complex LO plans [36][37]. However, it is not easy to realize wideband PLLs in deep sub-micron technologies because bulk CMOS technologies are optimized for highly integrated digital circuits and the highly conductive substrate degrades the quality (Q)-factor of passive components [38]. Moreover, the large parasitic capacitances of drain/source areas make it difficult to increase the oscillation frequency and the tuning range of VCOs. Especially, switches to control capacitor banks are critical because they determine the capacitance variation range of the capacitor banks.

Figure 6.1 shows a typical PLL with a wideband VCO. To increase the total frequency range of the VCO, a capacitor bank is generally adopted and many transfer curves are generated by changing capacitance because voltage tuning range is limited by supply voltage. The total frequency range of the VCO is given by

$$F_{range} = K_{vco} \cdot \Delta V_{tune} \cdot 2^N \qquad (22)$$

, where K_{vco}, ΔV_{tune}, and N are VCO gain, tuning voltage range, and the bit number of the capacitor bank, respectively. As the minimum pitch size of a transistor is scaled down,

the supply and threshold voltages are also scaled down with thinner oxide layers. Since the tuning voltage range is proportional to the supply voltage, the total frequency range also decreases as scaling down is accelerated. Thus, the dynamic range reduction means the total frequency range reduction. The phase noise of the VCO is also degraded because the signal power level also limited by the supply voltage. Therefore, the way to overcome the reduce frequency range and the degraded phase noise are critical issues of CPPLL design in deep sub-micron technologies.

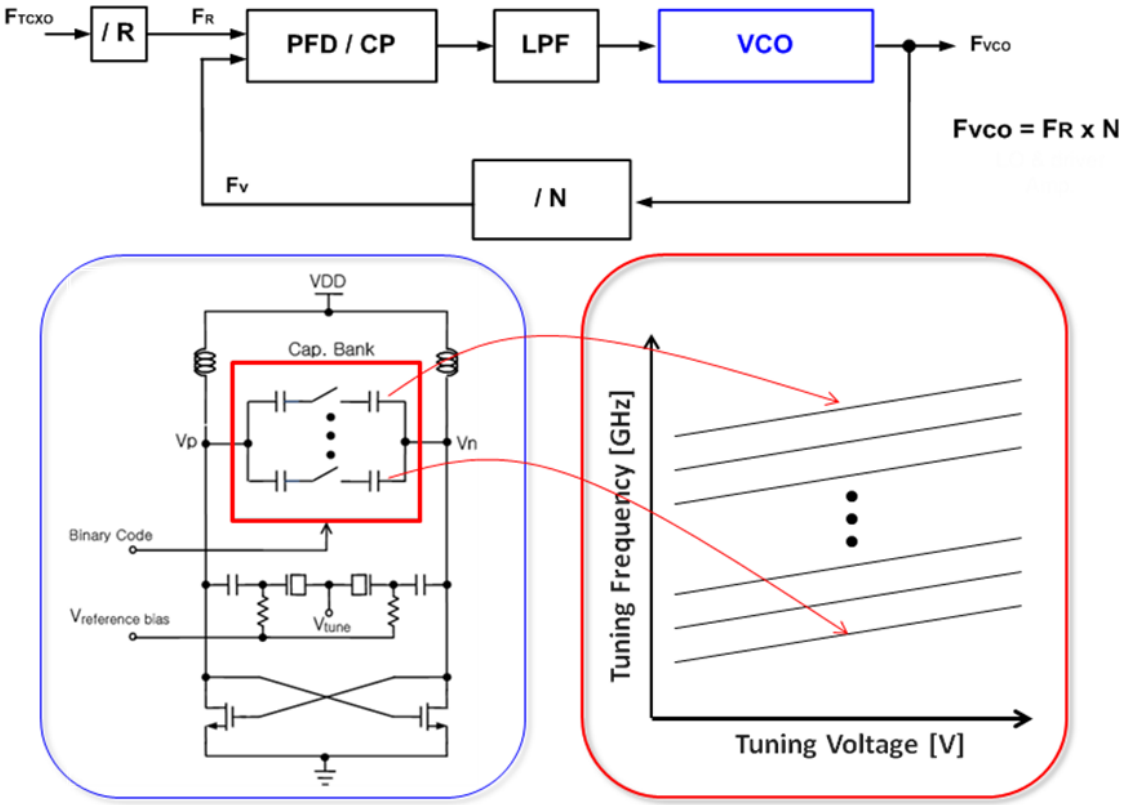


Figure 6.1. A phase-locked loop with a wideband LC-VCO.

In this chapter, a CPPLL with a wide frequency range is presented. The proposed PLL uses a 45nm SOI-CMOS technology, so the parasitic capacitance of a capacitor bank can be minimized, increasing the frequency range of the PLL [39].

6.2. Prior Arts

To increase the reduced frequency range due to supply voltage scaling down, multiple VCOs can be used and each VCO covers a specific frequency range or band. Another approach is to use complex LO plans to generate different ranges of frequencies from a single VCO. In this chapter, two typical cases are studied as prior arts.

6.2.1. PLL with Multiple VCOs

The simplest way to cover a wide frequency range is to use multiple VCOs as shown in Figure 6.2, containing a high band VCO for 7~10 GHz range and a low band for 4~7.2 GHz [36]. The 45-nm deep sub-micron technology enables to increase the high VCO frequencies up to 10 GHz. But the tuning range is less than 40 % due to parasitic capacitance. As the oscillation frequency increases, the influence of parasitic capacitance on frequency range is critical. Even though the application frequency range is from 0.1 to 5 GHz, higher frequencies are generated in the VCOs to utilize a simple LO plan, which only uses cascade of divide-by-2 circuits to generate IQ signals, without using analog intensive blocks such as polyphase filters and *Single-Side Band* (SSB) mixers.

The advantage of this architecture is that a simple LO plan is possible to cover the wide frequency range. But, the hardware increment due to two VCOs is a big drawback

in IC design. The low Q-factor of the inductors is also limiting the phase noise performance of the VCOs.

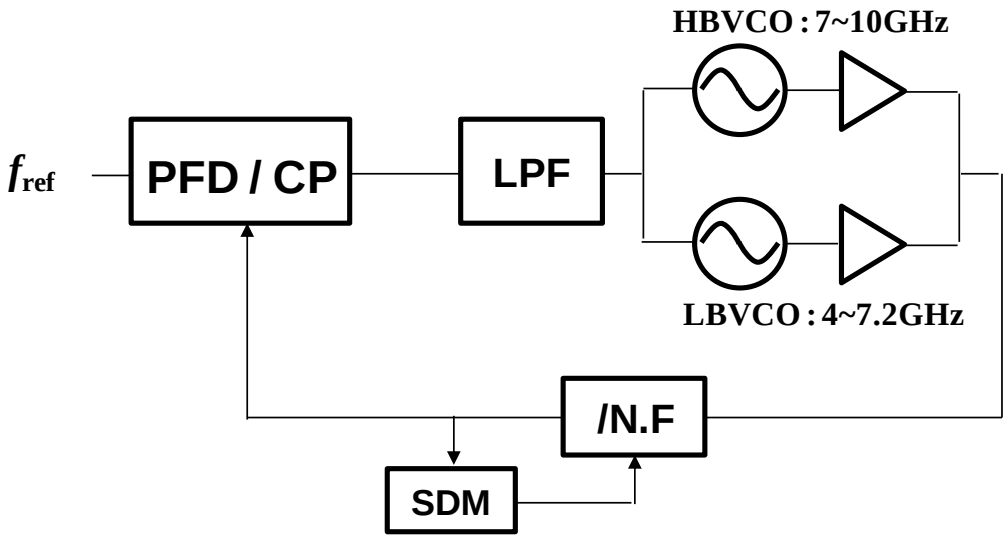


Figure 6.2. High and low band VCOs to cover 0.1~5 GHz frequency of a soft defined radio (SDR) receiver.

6.2.2. LO Generation Architecture with a Regenerative Loop

With a narrow VCO frequency range of 8.09~9.6 GHz, a multi-standard LO generation block covers the WiFi bands 2.4~2.5 GHz, 4.8~5.8 GHz, WiMax 2.3~2.7 GHz and 3.3~3.8 GHz [37]. As shown in Figure 6.3, the architecture includes a regenerative loop to generate low band (2.3~2.7 GHz) and mid band (3.3~3.8 GHz) signals. Additionally, a feed-forward path is also used for high band (4.8~5.8 GHz) signals. Two SSB mixers choose upper or lower band depending on required frequencies and prevent incorrect lock. This LO plan makes the VCO oscillate at non-integer multiples of the PA output frequency to overcome the frequency pulling effect. Spur

performance is a critical specification of LO design. Signal shaping technique, using triangle waveform signals as inputs of mixers instead of square waveform signals, improves spurious tone property by reducing harmonic components.

The advantage of the architecture is that the single VCO can cover a very wide frequency range with a smart frequency plan even though the VCO itself shows a very narrow frequency range. The high immunity to the VCO pulling effect is another good point of this architecture. However, the architecture is so complicated with many components, resulting in large hardware complexity and large area. Spurious tone performance will be degraded because mixing operation generates another source of spurious tones.

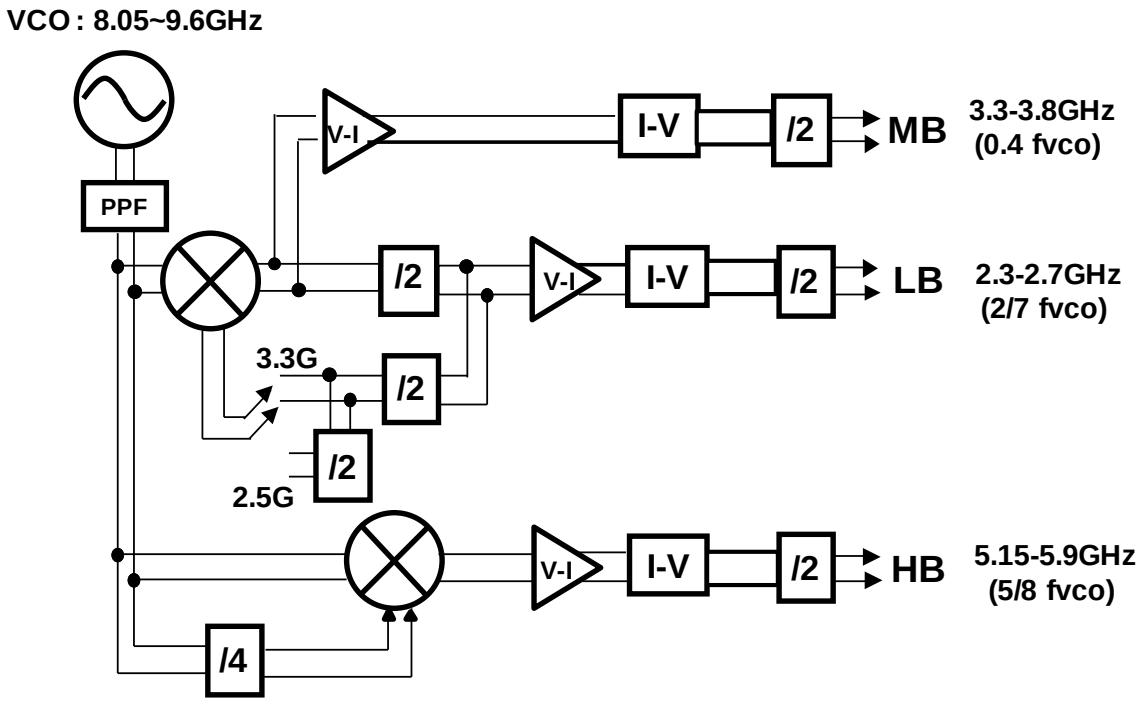


Figure 6.3. LO plan with a regenerative loop.

6.3. Design Strategy

The design goal of this research is to maximize the frequency range and to compensate the degraded phase noise performance. The phase noise is closely related to the Q-factor of the inductor used in a LC-tank. In this design, the oscillation frequency of the VCO has been increased because of two reasons. First, die area can be saved by using a smaller inductor. And second, high Q-factor can be obtained because the Q-factor of inductor is proportional to the oscillation frequency as shown in Figure 6.4. The oscillation frequency of the VCO can be expressed by

$$F_{OSC} = \frac{1}{2\pi \cdot \sqrt{LC}}$$

$$C = C_{fixed} + C_{variable}$$

$$= C_{fixed} + C_{min} \sim C_{fixed} + C_{max} \quad (23)$$

, where *L* and *C* are inductance and capacitance of a VCO, respectively. The capacitance consists of two part, fixed capacitance and variable capacitance. The fixed capacitance is the sum of the parasitic capacitances of switching transistors, inductor, routing metal lines, and fine tuning varactors. Variable capacitance is contributed by the on/off capacitance of the capacitor bank. The minimum capacitance, C_{min}, and the maximum capacitance, C_{max}, of the capacitor bank are determined in according to the control voltage of the MOS switches in the capacitor bank as shown in Figure 6.5. The C_{min} is closely related to the parasitic capacitance between drain/source and bulk. C_{max} corresponds to the lowest frequency and C_{min} to the highest one. Since the total frequency

range is highly dependent on the C_{max}/C_{min} ratio, the ratio should be maximized to increase the total VCO frequency range.

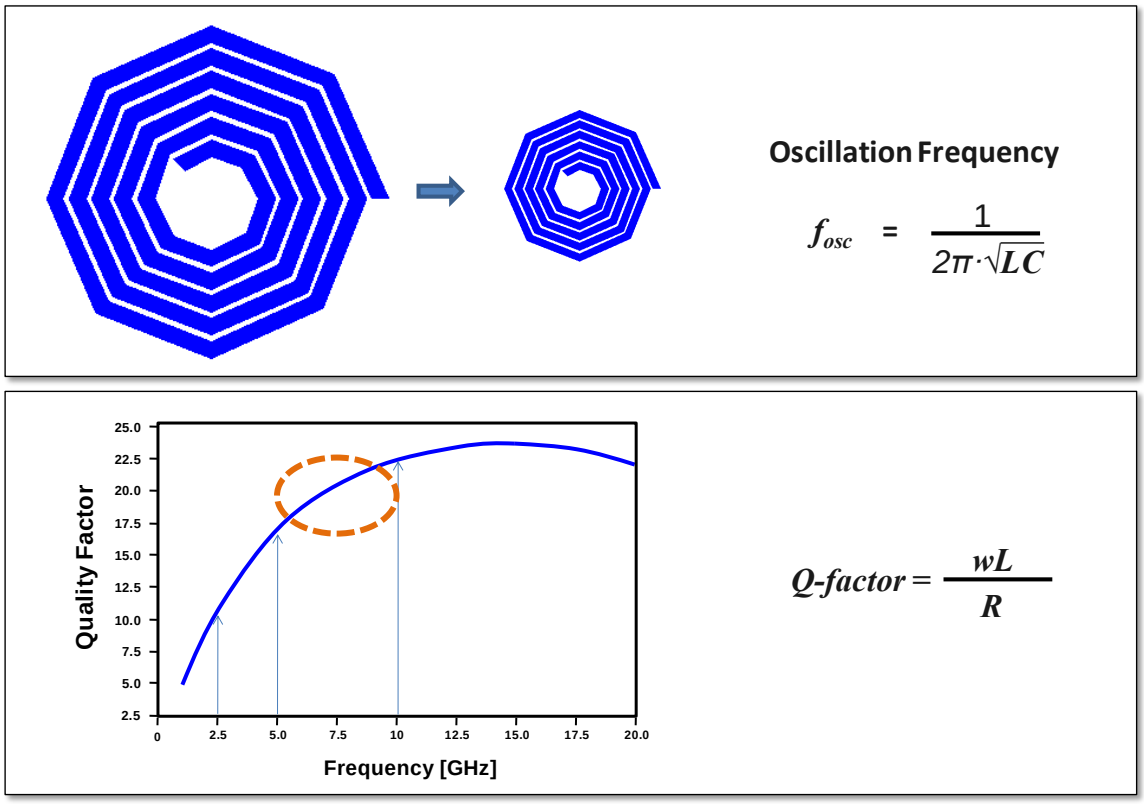


Figure 6.4. Small size and high quality factor inductor with a high oscillation frequency.

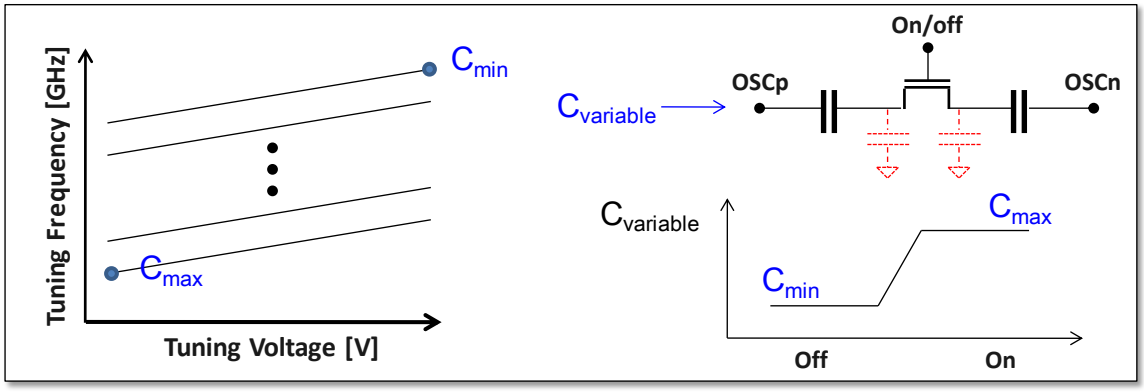


Figure 6.5. Frequency range and variable capacitance of the switched-capacitor bank.

Figure 6.6 shows three possible switches consisting of PN-junction varactors, AMOS varactors, or MIM capacitors with a MOS switch. Since AMOS varacotrs have higher C_{max}/C_{min} ratio than MIM capacitors with a MOS switch, the best choice for wide frequency range is the AMOS varactors.

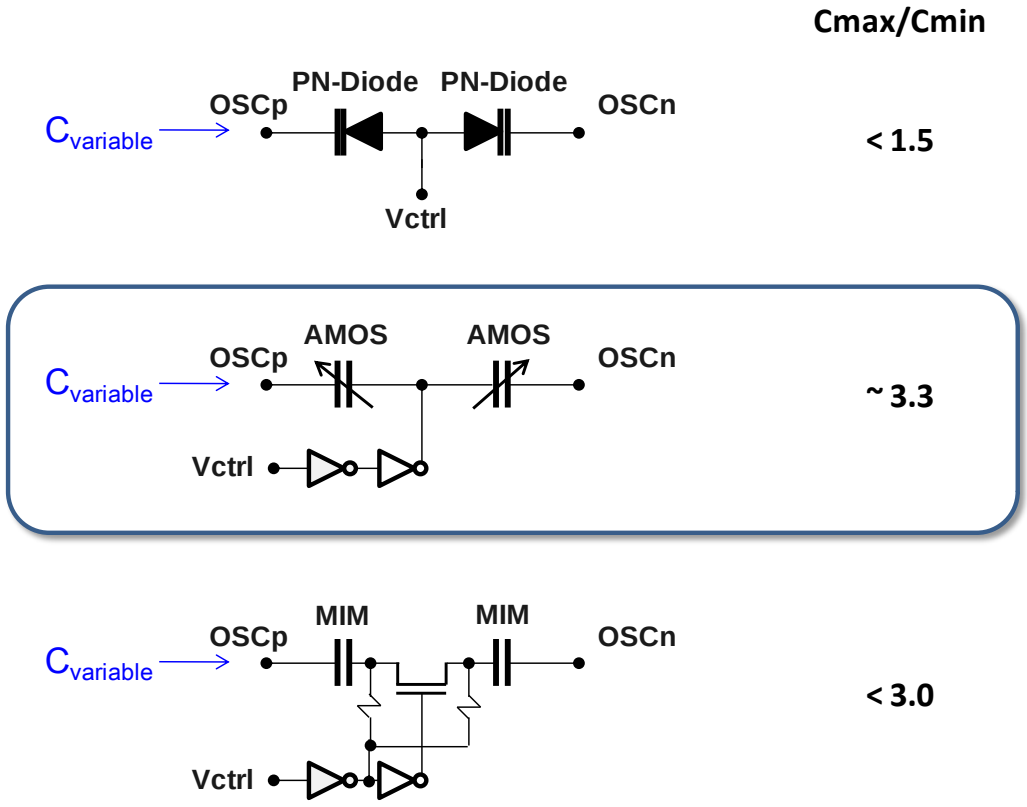


Figure 6.6. Switches for capacitor banks in bulk CMOS process (180-nm @2GHz).

In a SOI-CMOS technology, the Q-factor of passive components is higher than that of a bulk CMOS technology due to the higher resistance of substrate and a buried oxide layer. Since the buried oxide layer and *Shallow Trench Isolation* (STI) separate source/drain regions from the substrate as shown in Figure 6.7, the parasitic capacitance can be reduced significantly. Therefore, the MOS devices using SOI processes are highly

desirable for the switches of wideband VCOs, because of the higher C_{max} to C_{min} ratio of the capacitor bank. As shown in Figure 6.8, the reduced parasitic capacitance increases C_{max}/C_{min} ratio by reducing the C_{min} value. Figure 6.9 shows the simulation results of C_{max}/C_{min} of each switch in a 45nm SOI-CMOS process. Contrary to the bulk CMOS technology, the MIM capacitors with a MOS switch show much higher C_{max}/C_{min} ratio than the AMOS varactors.

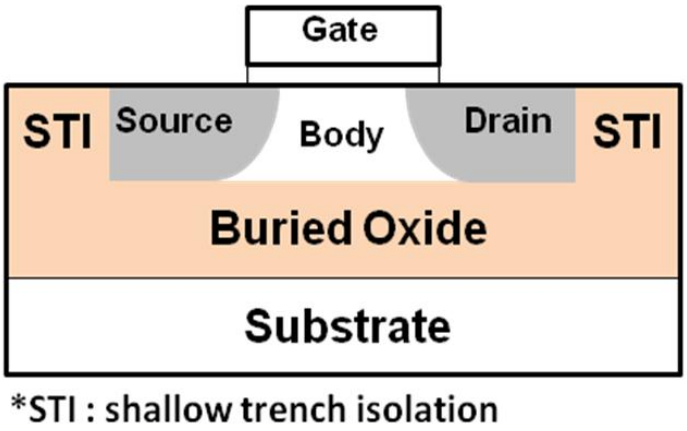


Figure 6.7. A MOS device structure in a SOI-CMOS technology.

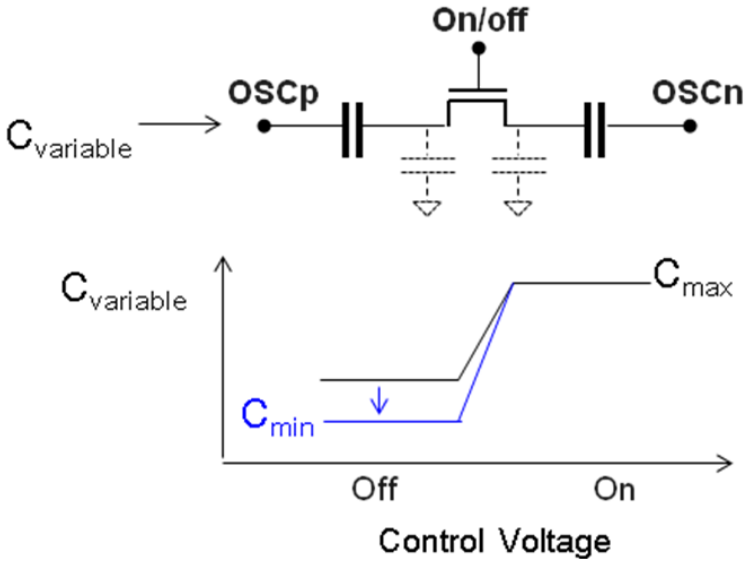


Figure 6.8. Parasitic capacitance reduction effect on the variable capacitance in a SOI-CMOS technology.

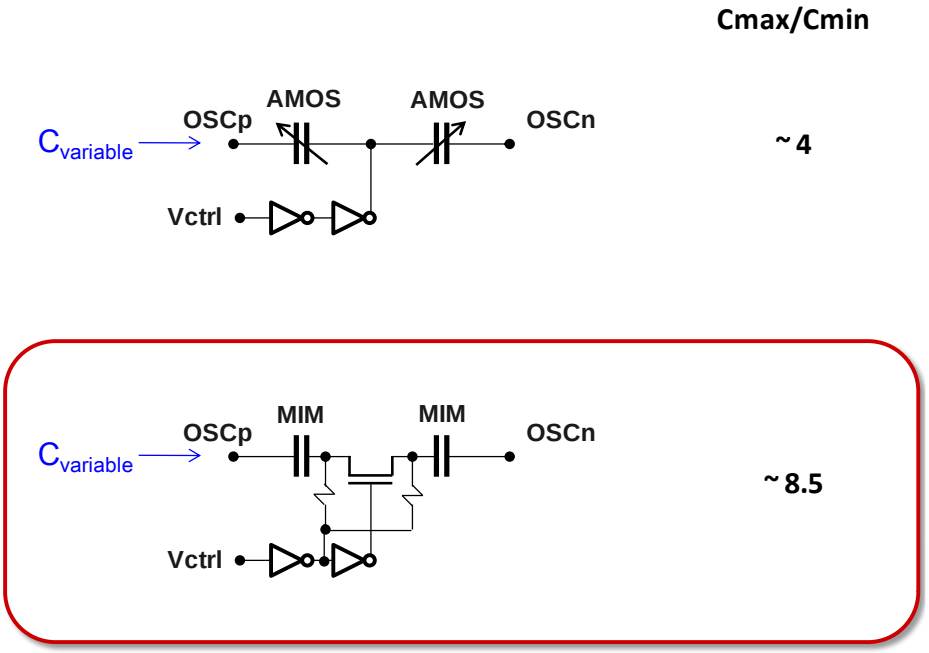


Figure 6.9. Switches for capacitor banks in SOI-CMOS process (45-nm @10GHz).

Frequency coverage is given by

$$Frequeny\ Coverage\ (\%) = \frac{F_{max} - F_{min}}{F_{center}} \times 100 \qquad (24)$$

, where F_{max}, F_{min}, and F_{center} are maximum, minimum, and center frequencies of the VCO, respectively. If the VCO is designed to cover from 5GHz to 10GHz, the frequency coverage should be 66.7%. And the PLL can cover a continuous frequency range from 625MHz to 10GHz with simple divider-by-2 circuits.

However, a very high C_{max}/C_{min} ratio is required with very small parasitic capacitance to realize this system. Figure 6.10 shows the relationship between C_{max}/C_{min} ratio and frequency coverage. With 600pH inductance and 0.1pF fixed capacitance, the

simulation result shows that more than 4.75 ratio is required to obtain 67% coverage. But it is not easy to realize more than 4 with a bulk CMOS technology. Also, the influence of fixed parasitic capacitance on frequency coverage is critical. With 600pH inductance and 4.5 C_{max}/C_{min} ratio, Figure 6.11 shows that less than 40fF fixed capacitance is required to have 67% coverage. Compared with sub-micron technologies, the 45nm process has a benefit of small parasitic capacitance because smaller switching transistors can supply enough negative resistance to the LC-tank with smaller threshold voltages. SOI technology also enables to achieve a large C_{max}/C_{min} ratio because of small parasitic capacitances in MOS devices. Therefore, the 45nm SOI-CMOS technology provides low parasitic capacitance and high C_{max}/C_{min} ratio.

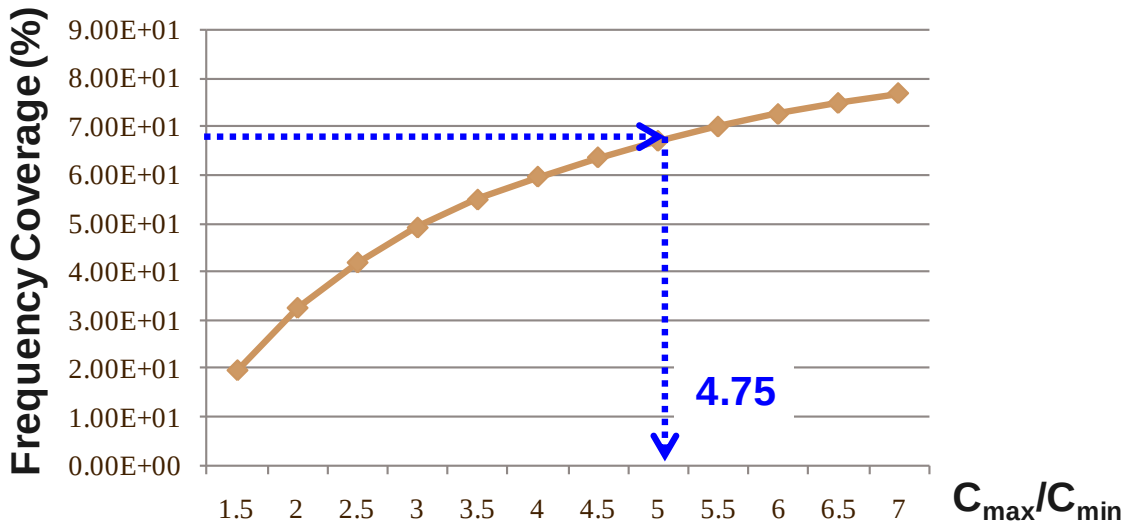


Figure 6.10. Simulation results of frequency coverage vs. *Cmax*/*Cmin* ratio.

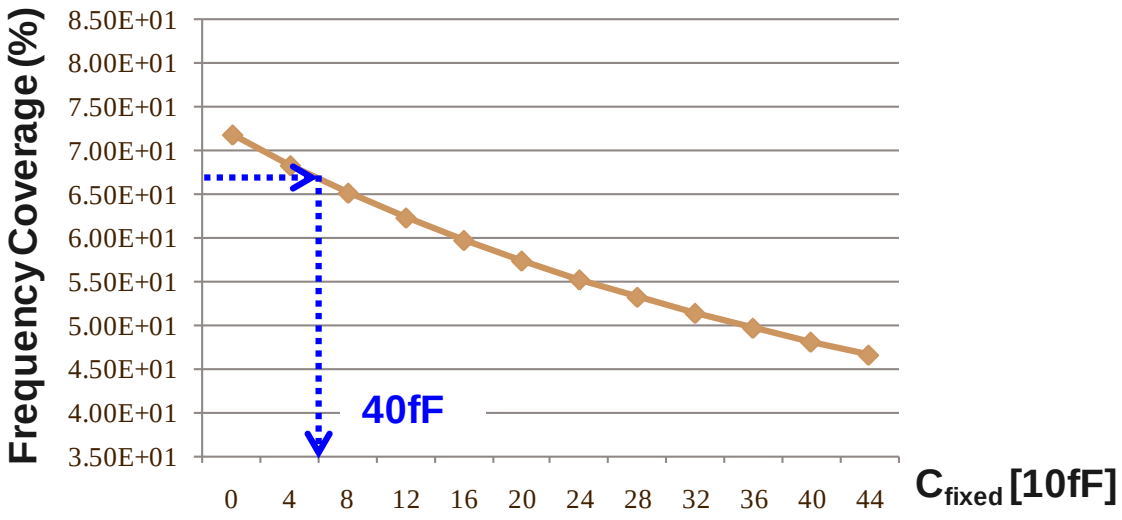


Figure 6.11. Simulation results of frequency coverage vs. fixed capacitance.

6.4. Wideband Phase-Locked Loop

A simplified block diagram of the proposed PLL with a wide band LC-VCO is illustrated in Figure 6.12. The PLL consists of a wideband VCO, buffers, a phase-switching prescaler, dividers, a PFD/CP, and a passive loop filter. The VCO generates 4.875~9.65 GHz frequency signals in the VCO core. 4 different phase signals of 1.22~2.41 GHz are created through buffers and divide-by-2 circuits. A 4/4.5 divider realizes 0.5 division ratio using the phase-switching technique [40]. The signals are finally fed back to the PFD. The PFD/CP generates continuous pulse trains and force to lock after a certain time. A reference signal is supplied from an off-chip VCTCXO for high spectral purity. A third order 3-bit DSM is used to realize fractional frequency division ratio. The noise boosting from the DSM has been suppressed enough to be below the VCO phase noise level. The third order sample-hold loop filter proposed in Chapter 5 is used in this PLL to improve the in- and out-of-band phase noise and reference spur level for high spectral purity. Entire PLL block operates with 1V supply. Analog and digital powers and grounds are separated for noise performance.

To support multiple standards, a simple LO plan is suggested as shown in Figure 6.12. For high frequency applications, the signals from VCO buffers are directly used for LO signals or carriers for transmission, while the output signals of the devider-by-4 block are exploited for low frequency applications. Since the frequency range of the VCO is wide enough to cover almost all cellular standards from 623MHz to 10GHz, there is no need to use multiple VCOs or complex LO plans. Only one of two paths is activated depending on the applications.

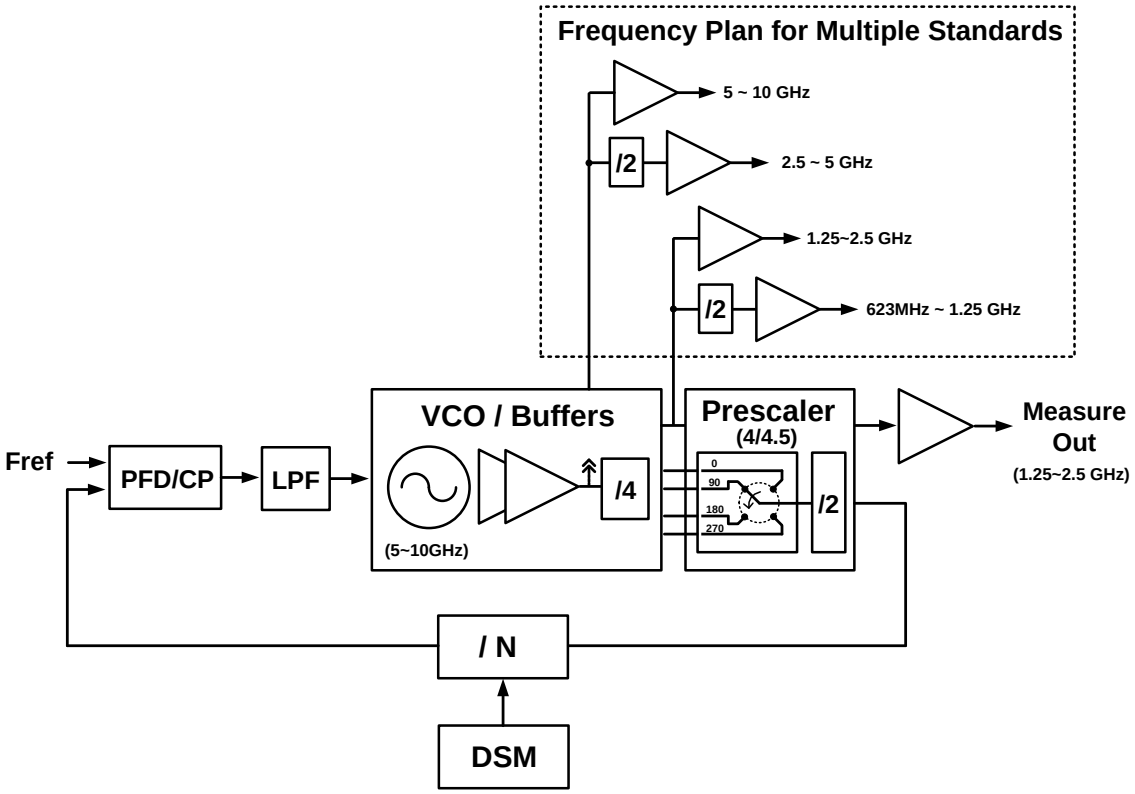


Figure 6.12. Block diagram of the proposed PLL with a wideband VCO and a simple frequency plan for multi-standards

6.4.1 Wideband Voltage-Controlled Oscillator and Buffers

Figure 6.13 shows the proposed wideband VCO. The VCO incorporates a spiral inductor, a capacitor bank, a fine tuning varactor, and a current control block. To maximize the C_{max}/C_{min} ratio and simplify the structure, a CMOS type VCO core is employed. With this architecture, any blocking capacitors and biasing circuits between oscillation nodes and the capacitor bank (or the AMOS varactor) are not used. The binary-weighted capacitor bank is controlled by a 6-bit digital code. The small spiral inductor is used to generate higher oscillation frequencies to save area. The minimum

controllable capacitance per bit is as small as 40-fF. Thanks to the excellent matching characteristic of deep sub-micron technology, the monotonicity of the capacitor bank is guaranteed. The tuning range of the analog AMOS varactor is set to cover the frequency range of two *Least Significant bits* (LSBs) to ensure stable frequency locking. Since a 6-bit capacitor bank is used to cover wide frequency range, the frequency difference between two adjacent curves and the VCO gain increase with oscillation frequency. Figure 6.14 is a simulation result of a 5-bit capacitor bank. The PLL bandwidth also changes. Therefore, it is necessary to control the PLL bandwidth to compensate the variation due to oscillation frequency change.

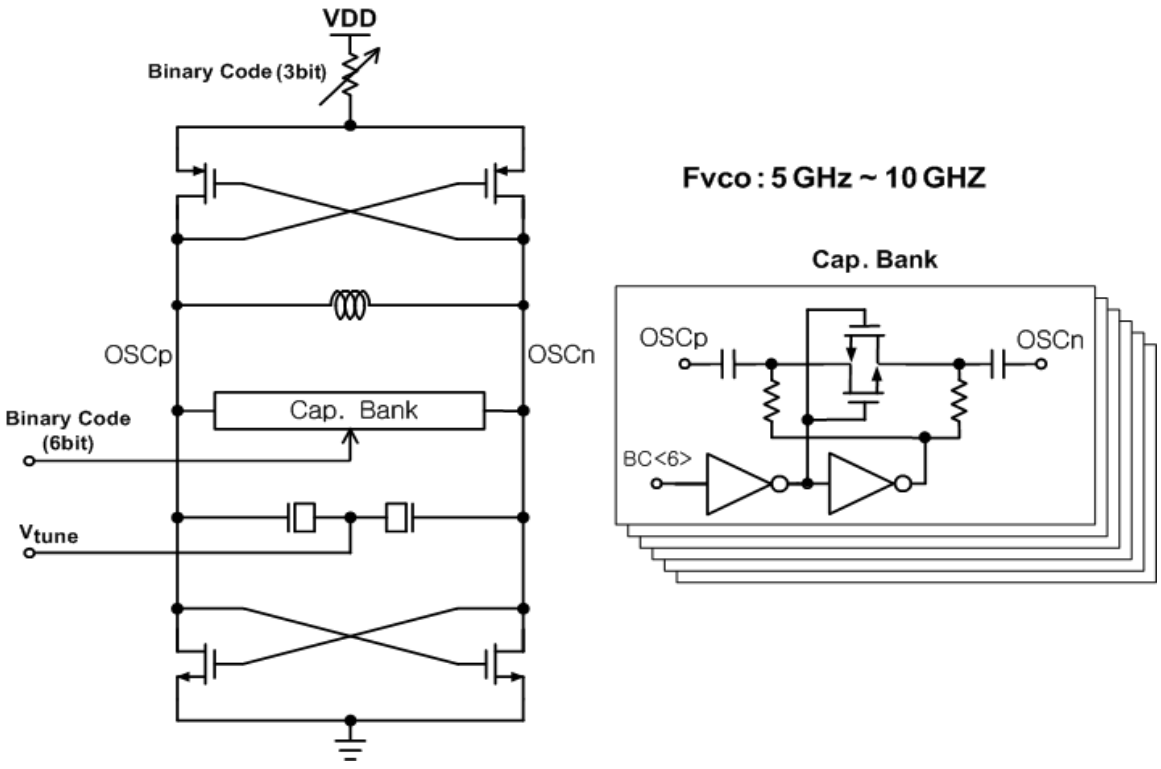


Figure 6.13. LC VCO with a wide frequency range. 6-bit capacitor bank covers 5GHz frequency range.

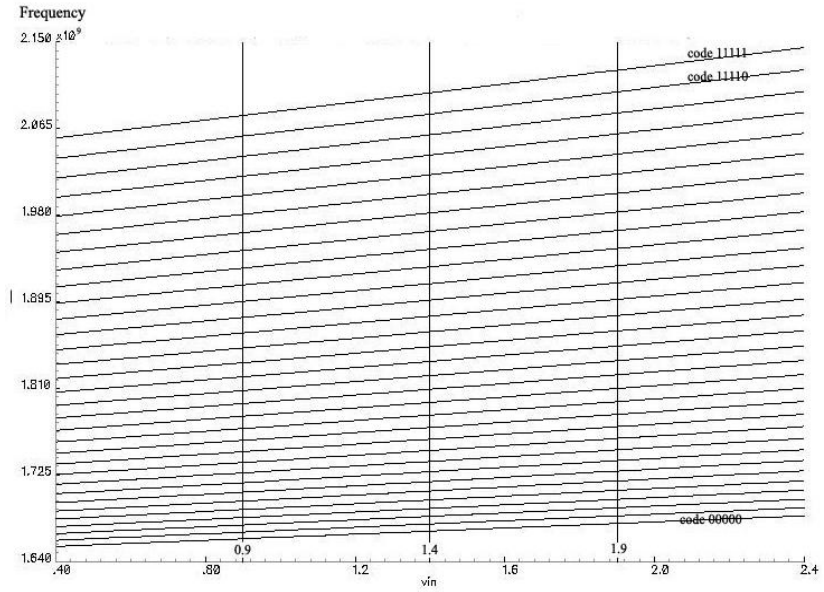


Figure 6.14. System simulation result of a 5-bit capacitor bank. The frequency difference between two adjacent curves and VCO gain increase with oscillation frequency.

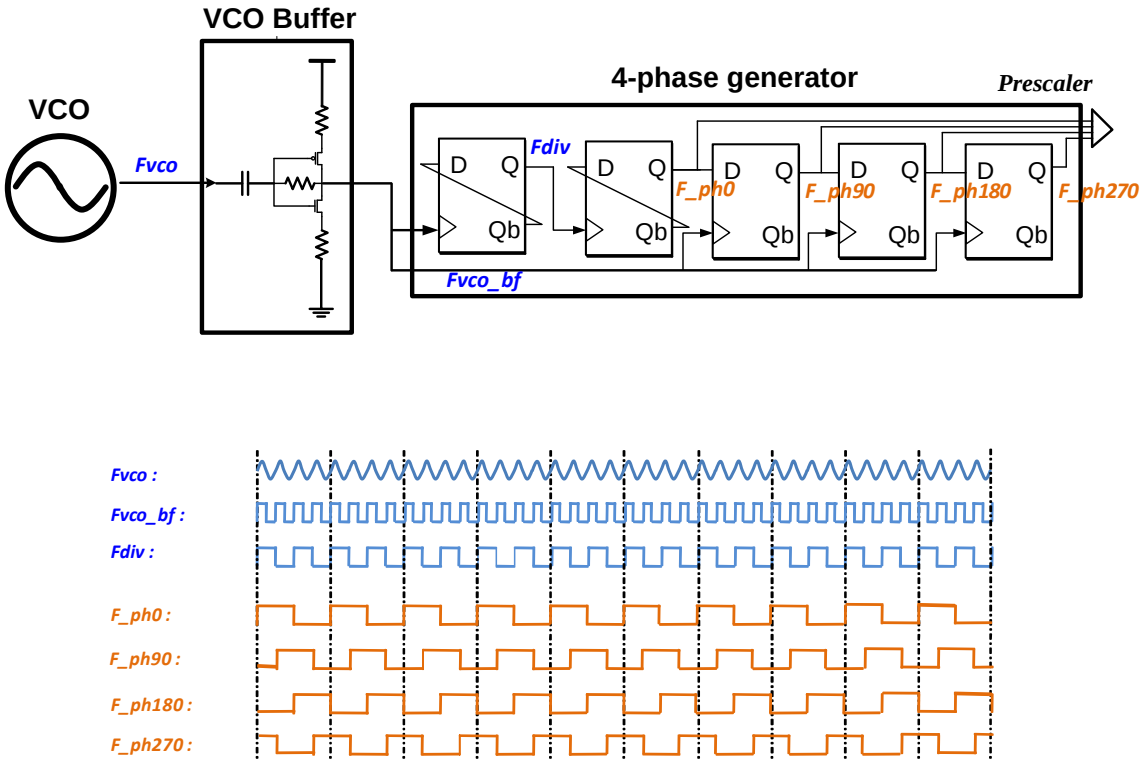


Figure 6.15. VCO buffers and 4-phase signal generation.

Figure 6.15 shows the VCO signal path from the VCO core to the prescaler. The VCO output signals go into a 4-phase signal generator after a VCO buffer. Since the prescaler use 4-different phase signals, the 4-phase signal generator is required. The VCO output signals are divided by 4 and three cascaded D flip-flops are used to generate 4 phase signals.

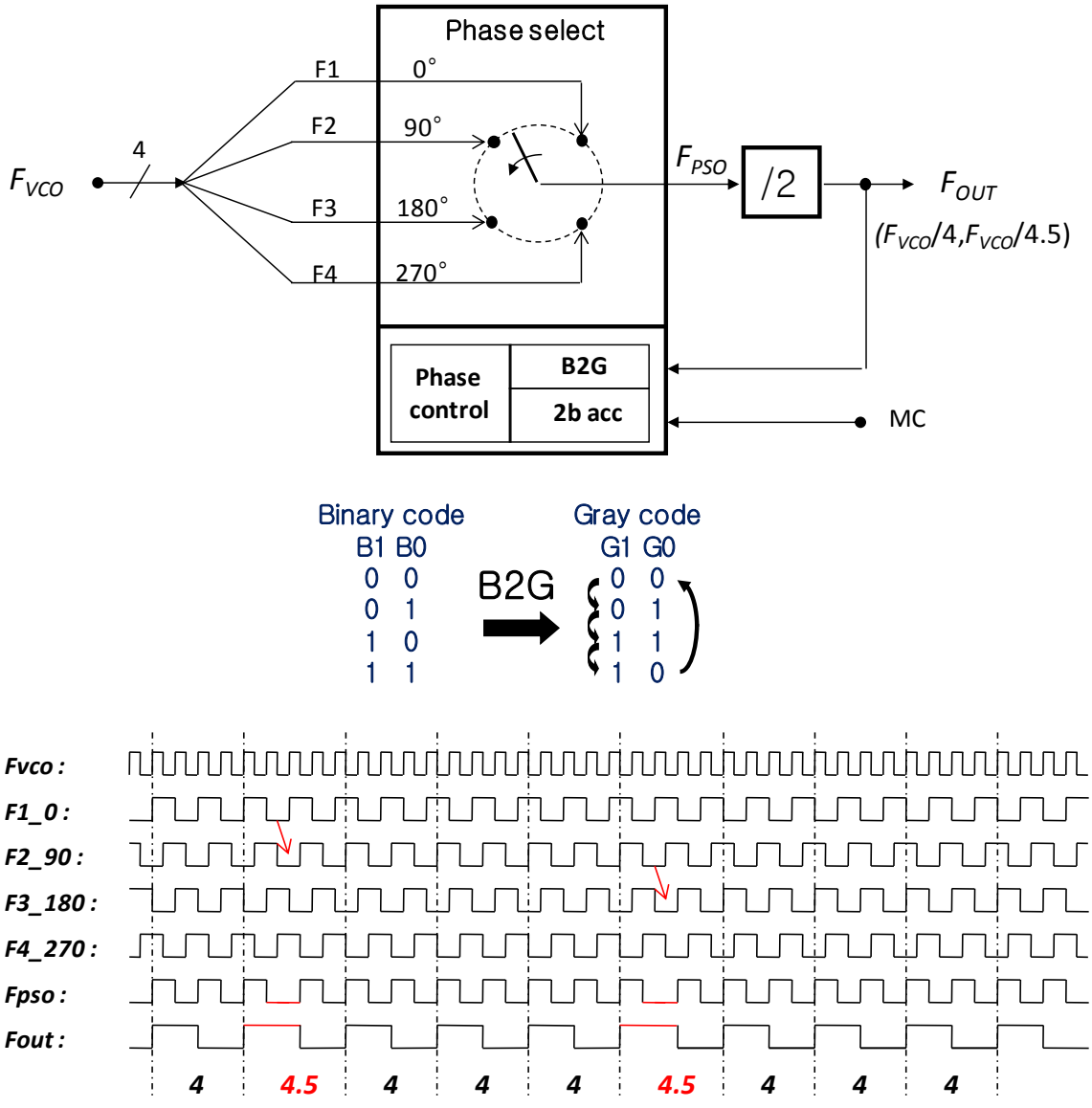


Figure 6.16. Phase switching type prescaler and timing diagram of main signals.

6.4.2 Prescaler

Figure 6.16 shows the phase switching type prescaler and timing diagram of main signals [40]. It consists of a phase selection block, an accumulator, a binary-to-gray code converter, and a phase controller. Whenever new MC signal comes in, the accumulator generates a binary code and it is converted to a gray code through the B2G block. Based on the current state and input signal, the phase controller determines whether the phase of the output signal to be switched or not. The phase selection block chooses one of four signals and connects it to the output path. Each phase switching results in 90-degree phase increase. The timing diagram in Figure 6.16 illustrates phase switching points. The output signals have two transitions from phase 0 degree to phase 180 degree.

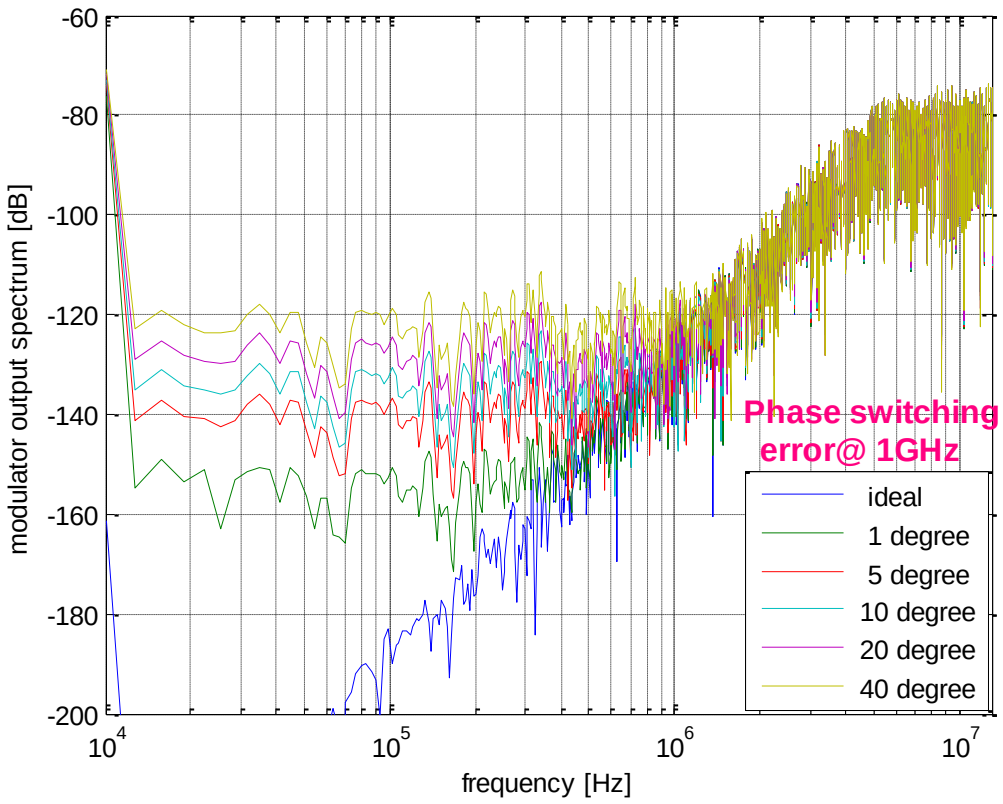


Figure 6.17. Noise folding effect due to phase switching error in a phase switching type prescaler.

The phase switching operation is performed in digital domain. Therefore, phase switching error is ignorable in circuit design level. However, careful layout skills are needed because the frequencies of 4-phase signals are 1GHz band, and asymmetric path delays can generate critical phase switching errors. Ideally, each transition increases an exact 90 degree of phase. But, the delay difference among four signal paths results in asymmetric duty cycle; more than 90 degrees or less than 90 degrees. This phase switching errors increase the noise folding effect in the FN-PLLs. The noise folding effect deteriorates the in-band phase noise of the FN-PLLs. Figure 6.17 is a simulation result of the phase switching error. The in-band phase noise degradation increases with phase switching error. Less than 5 degree phase switching error is required for the phase noise not to be degraded too much. The in-band phase noise degradation due to 5 degree is comparable to the 1% PFD/CP linearity error as you can see in Figure 6.18.

6.4.3 Phase Frequency Detector and Charge-Pump

PFD/CP nonlinearity is a critical issue in the FN-PLLs. As mentioned before, it is another source of the noise folding in DSMs. Figure 6.16 shows the noise folding effect due to PFD/CP nonlinearity. In the ideal case, the noise power of the DSM is so small that it can provide high SNR in the low frequency region. But the nonlinearity effect increases in-band phase noise level. Since very small linearity error like 5% results in huge in-band phase noise degradation, the linearity improvement technique is needed in the PFD/CP.

In this design, we tried to improve the PFD linearity by inserting a leaking current to introduce a static current offset in transfer curve of the PFD. Figure 6.19 shows the PFD/CP with the leaking current. This offset current moves the operating point of the PFD from zero-crossing point to linear region as shown in Figure 6.20. We don't have to care about the dead-zone problem with the leaking current. With the down leaking current, only U_p current is generated as shown in Figure 6.21. One concern about the leaking current is the level of reference spur. However, the reference signal spur is well suppressed because of the high operating frequency of the FN-PLLs.

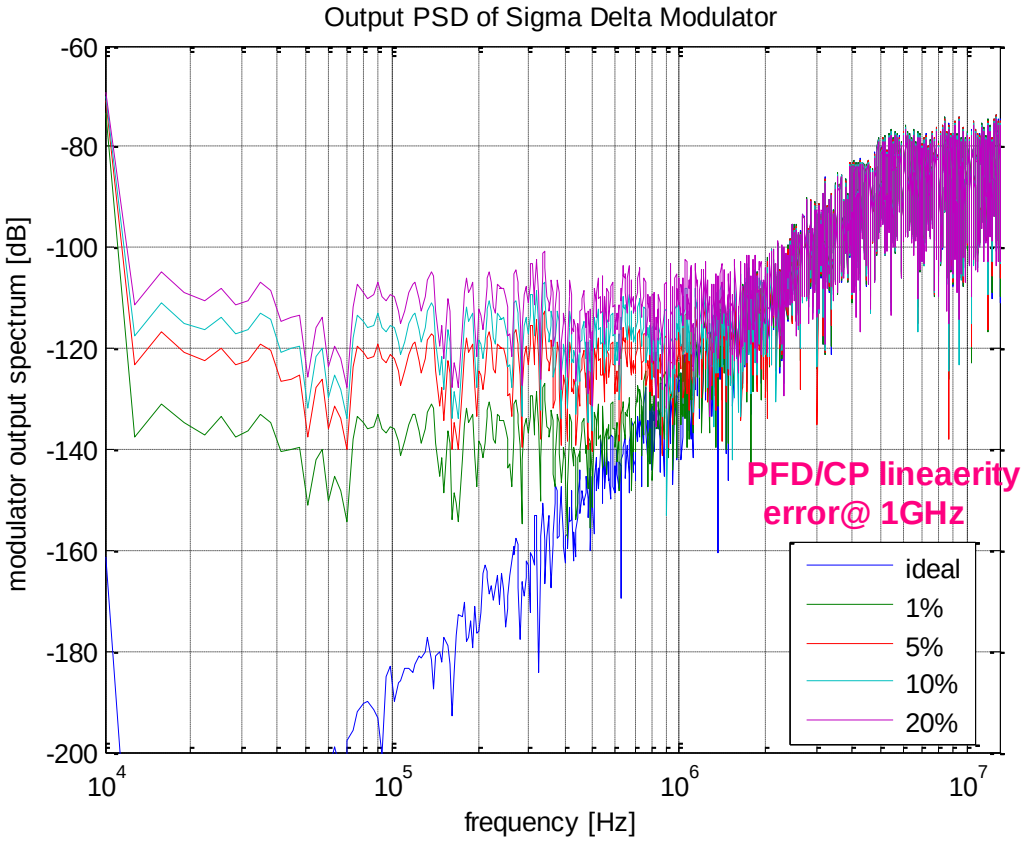


Figure 6.18. Noise folding effect due to PFD/CP nonlinearity.

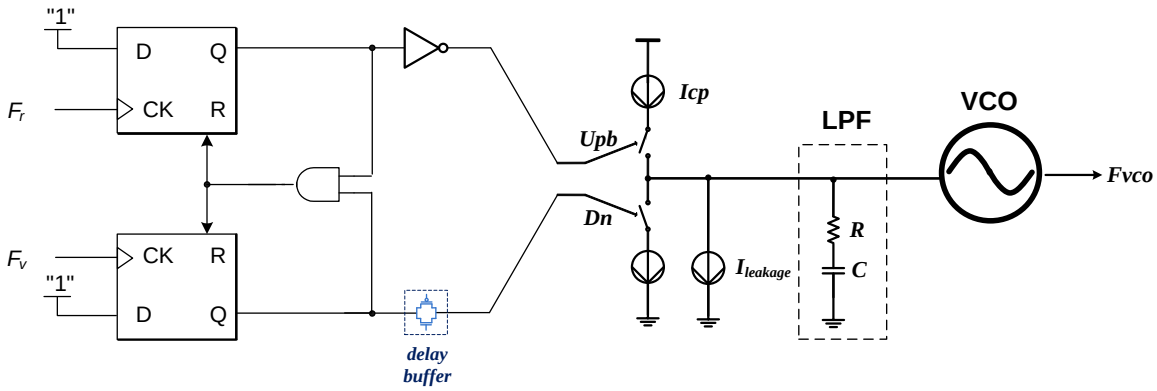


Figure 6.19. PFD/CP with a leaking current to insert a static current offset and a delay buffer to compensate the delay difference between two paths.

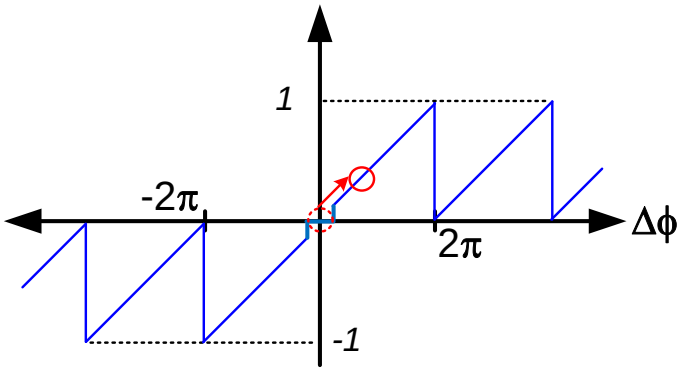


Figure 6.20. PFD operating point change due to the leaking current.

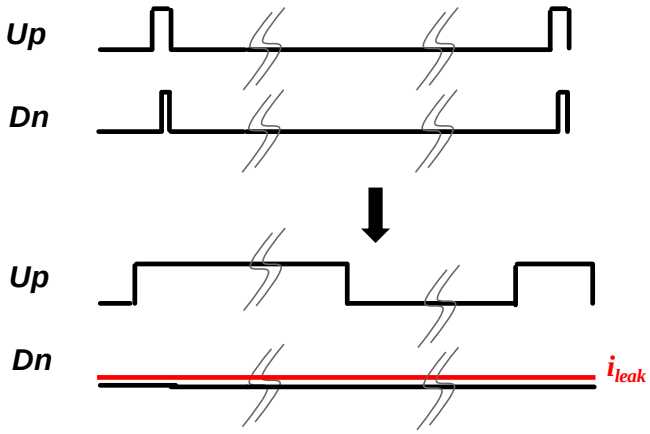


Figure 6.21. Only U_p current is generated with a leaking current.

To compensate the delay difference between two paths, a delay buffer is used. That is because the charging path is activated by the U_{pb} signal, while the sinking path is activated by the D_n signal.

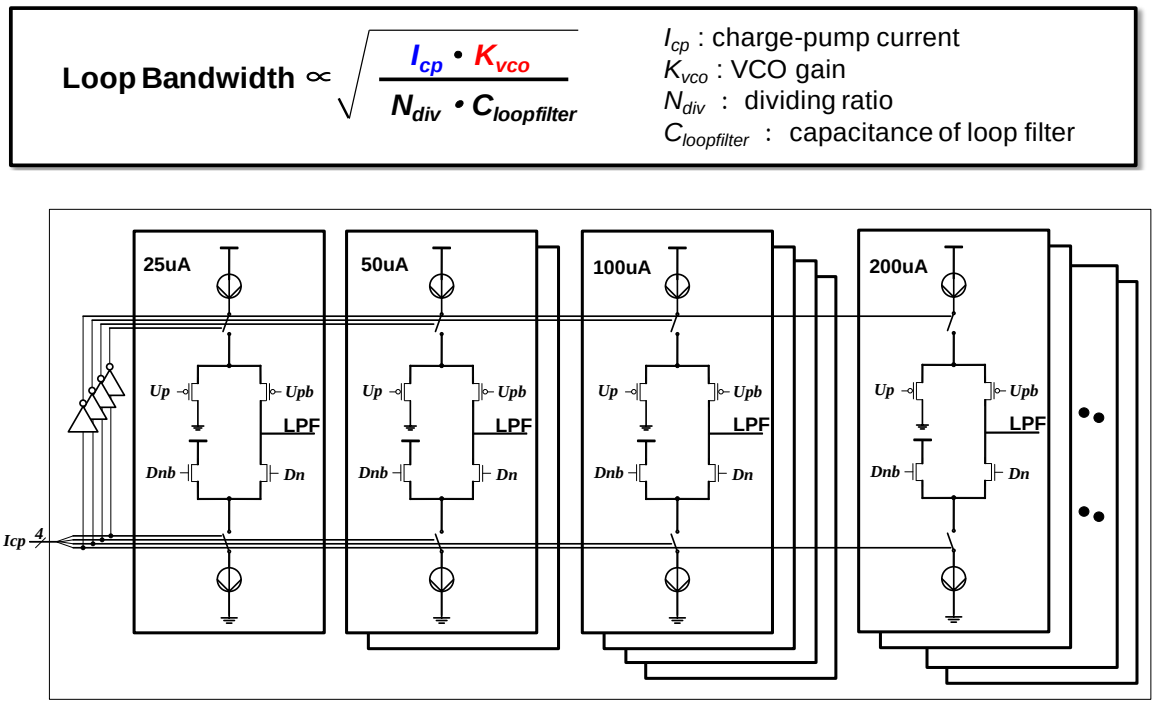


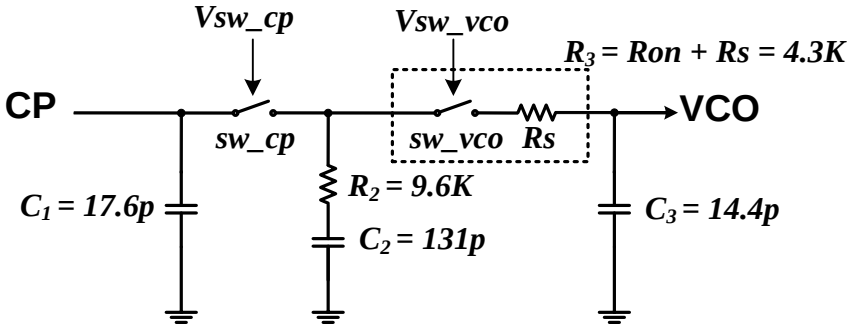
Figure 6.22. A CP block with a variable CP current control scheme.

Figure 6.22 shows a CP block used in this work. The same current values are sourcing at the top and sinking at the bottom of each branch. Since the current steering switches are utilized, the switching speed is fast. If we consider the PMOS network only, when a switch is turned off, the remained charge in the source region is drained to the other signal path quickly. And when the switch is turned on, the current source is charging the source region of the switch rapidly. To compensate the PLL bandwidth variation due to K_{vco} change, a programmable control scheme is used. A 4-bit digital signal determines the CP current. A 25-uA unit current cell is used and multiple cells are

activated for higher CP current. By doing this, the current control range is extended to 400 uA with a monotonic increment.

6.4.4 Loop Filter

The loop filter design is done with the help of a system simulation tool [41]. The PLL bandwidth of 160 KHz, phase margin of 47 degree, and default CP current of 75uA are selected as design parameters. The capacitance and resistance for each component are determined from these values. The R_3 value includes the turn-on resistance of *sw_vco*. The resistance value for R_3 can be minimized to reduce the thermal noise level as long as the third pole position is preserved. The value of R_3 is reduced to 4.3 KΩ and the C_3 value is increased to 14.4 pF. The designed LPF and all design values are shown in the Figure 6.23.



I_{cp} = 75uA	R_2 = 19.6K
K_{vco} = 30MHz/V	R_3 = 4.3K
F_{vco} = 2GHz	C_1 = 17.6pF
F_r = 52MHz	C_2 = 131pF
Bandwidth = 160KHz	C_3 = 14.4pf
Phase Margin = 47	

Figure 6.23. The designed LPF and all design values.

To make sure the enough suppression of the noise boosting due to the DSM, a system simulation with the designed LPF is done and the result is shown in Figure 6.24. In-band phase noise is dominated by PFD/CP, but out-of-band phase noise is degraded by the noise from VCO and DSM. The designed PLL suppresses the out-of-band phase noise boosting from the DSM to be below the VCO noise level.

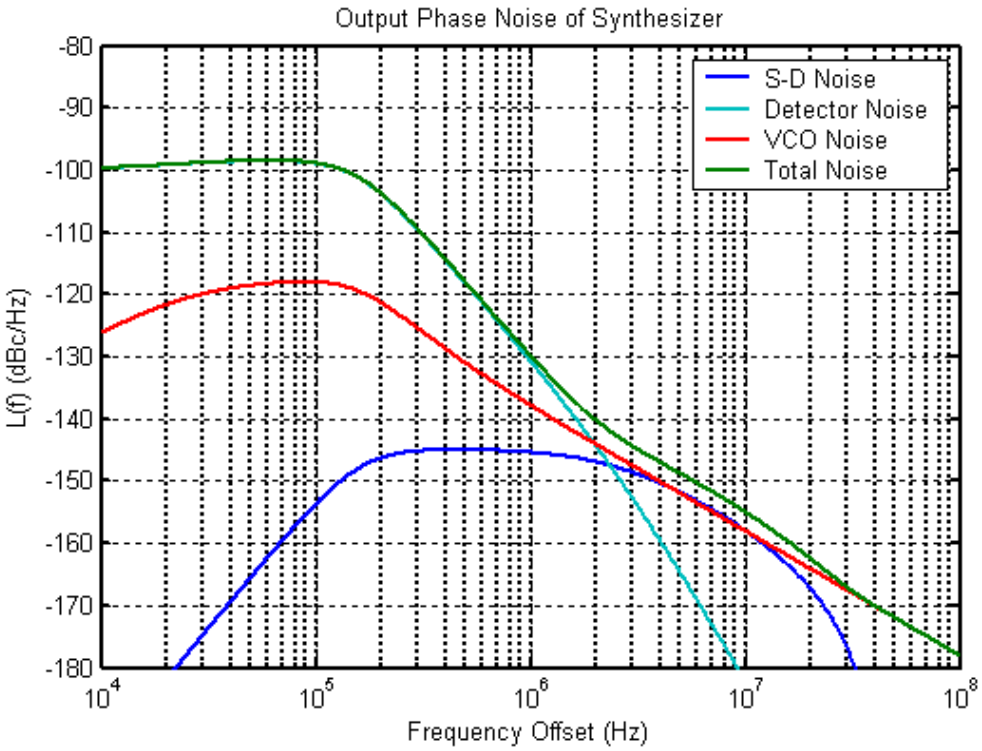


Figure 6.24. System simulation results with the designed LPF.

(*Simulation result using CPP sim of Perrott, M.H)

6.4.5 Delta-Sigma Modulator

A 3-bit third order DSM is used as shown in Figure 6.25. The DSM has three stages and each stage has an accumulator and an adder. A 3-bit quantizer is used at the

end of the DSM chain. The quantizer output is fed back to each stage. The feedback coefficients are used to determine the cut-off frequency of the noise transfer function of the DSM and to stabilize the DSM. The average value of the DSM output follows the input signal without any periodic tones. But the operating frequency should be high enough to minimize the error between the average value and the target value. The input of the DSM in the FN-PLLs has DC value because it is a channel frequency. A Simulink model is constructed to check the noise transfer function of the DSM. Figure 6.26 shows a Simulink model for the 3-bit third order DSM and time domain simulation result when -0.25 is applied as an input. The spectrum of the DSM and the out-of-band phase noise contribution from the DSM are shown in Figure 6.27.

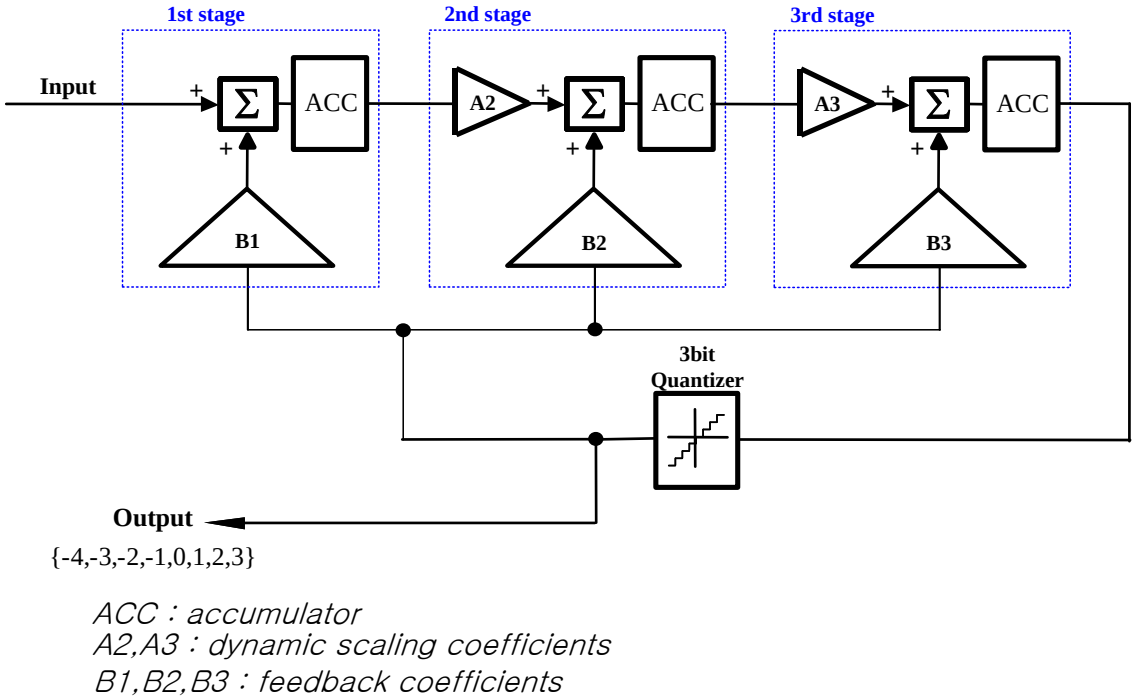
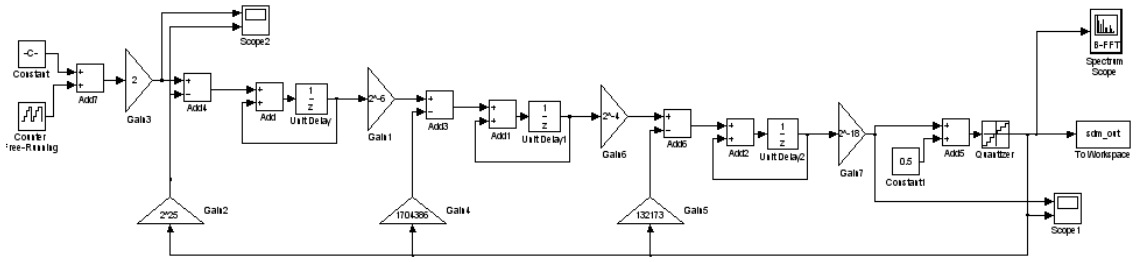
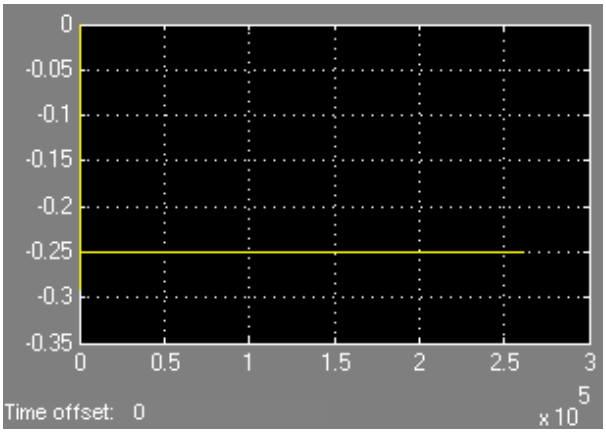


Figure 6.25. 3-bit third order DSM.

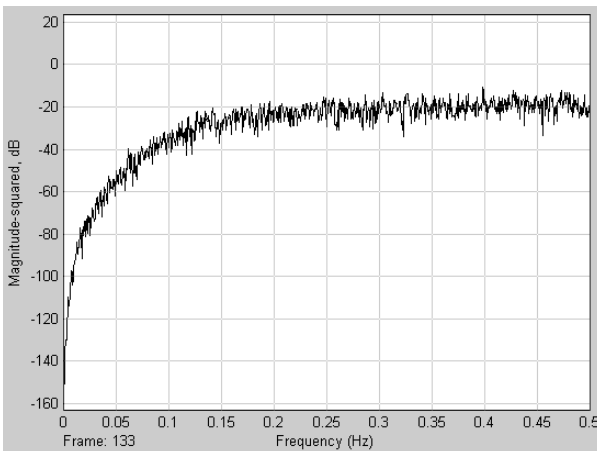


(a)

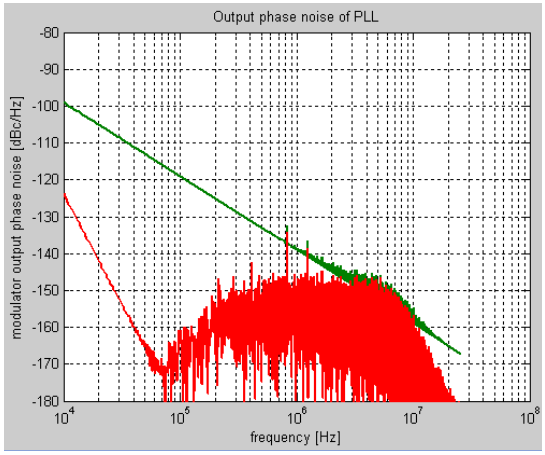


(b)

Figure 6.26. A Simulink model of the 3-bit third order DSM (a) and time domain simulation result (b).



(a)



(b)

Figure 6.27. System simulation results of a 3-bit third order DSM. Noise power of the DSM output (a) and out-of-band phase noise contribution from the DSM (b).

6.5. Measurement Results

The proposed PLL is designed and fabricated in a 45-nm deep sub-micron SOI-CMOS technology. The VCO frequency range is characterized under open-loop conditions. As expected, a very wide frequency range up to 4.78 GHz is supported with a single VCO. The tuning frequency is from 4.87 GHz to 9.65 GHz and the frequency coverage is 65.8%. The PLL can cover from 610MHz to 9.65GHz with the simple frequency plan except 90MHz range. Shown in Figure 6.28 is the measured frequency range according to each code when the tuning voltage is set to 0.5V. The code is inversely proportional to the capacitance of the capacitor bank. Therefore, the oscillation frequency increases with the code. Figure 6.29 shows fine tuning curves for each code depending on the tuning voltage. Each code has enough overlapping regions with adjacent codes to make sure stable locking.

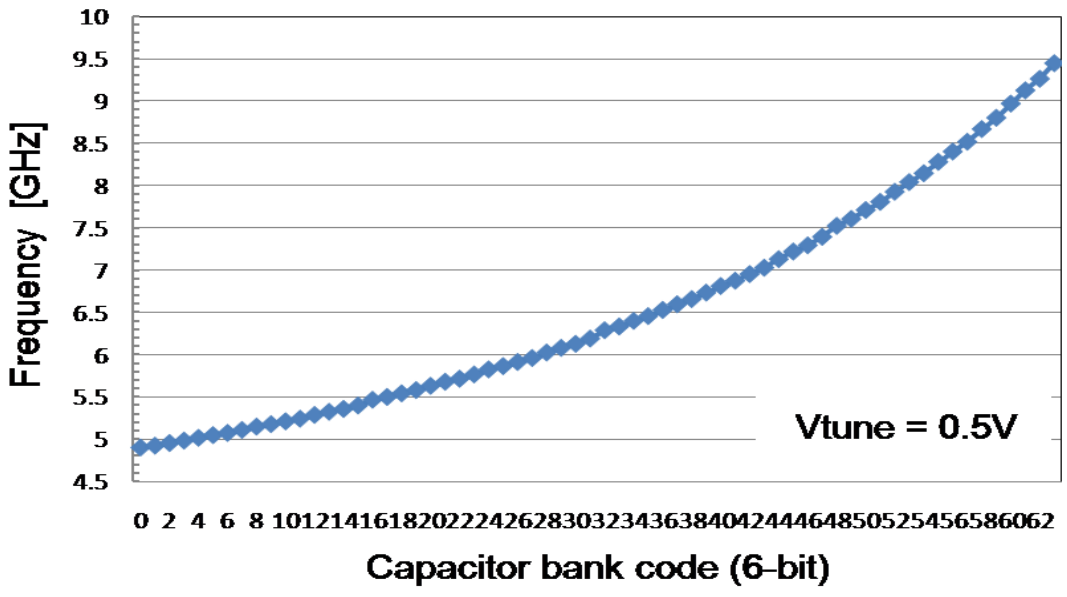


Figure 6.28. Measured frequency tuning range when Vtune is 0.5V.

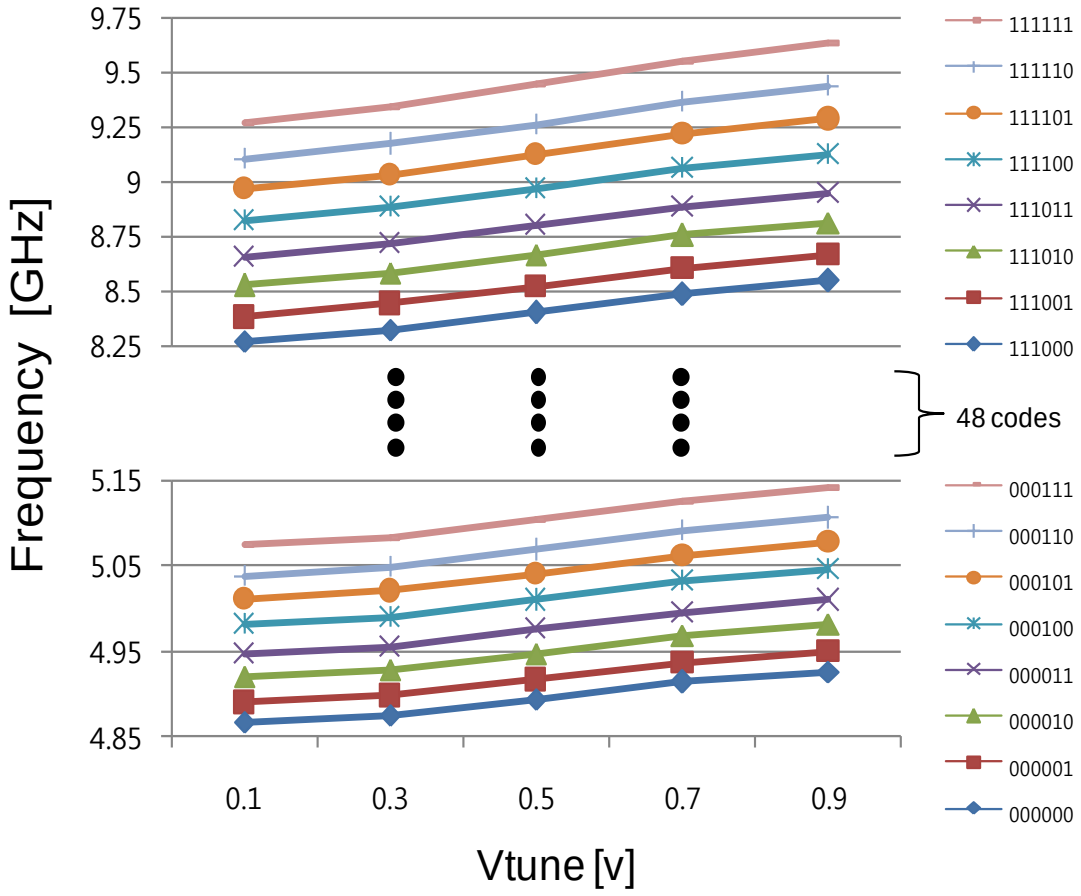


Figure 6.29. Fine tuning curves for each code depending on Vtune.

The measured frequency coverage is compared with the frequency ranges of published state-of-art LC VCOs as shown in Figure 6.30. As technology scales down to deep submicron, the frequency coverage reduces. As mentioned before, the *Kvco*/4 varies from 10 MHz/V to 90 MHz/V as shown in Figure 6.31. So, it is essential to control CP currents to obtain constant bandwidth over the frequency range. Figure 6.32 shows the bandwidth controlled by the CP currents. The minimum and maximum bandwidths are 40 KHz and 200 KHz with a carrier frequency of 1.248 GHz. The phase noises of the free-

running VCO are -108, -135, and -145 dBc/Hz at the offset frequencies of 100 KHz, 3 MHz, and 10 MHz as shown in Figure 6.33.

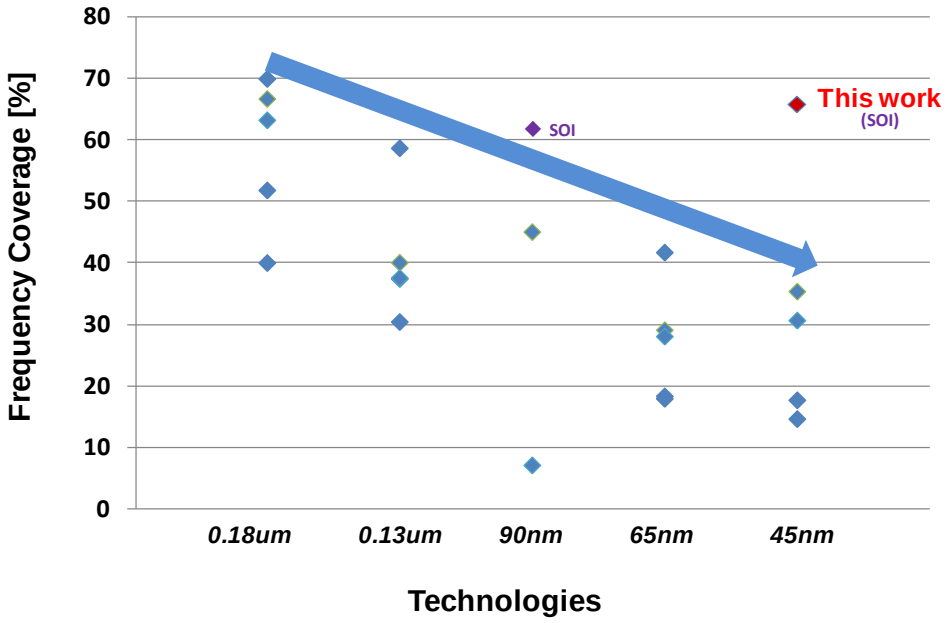


Figure 6.30. Performance comparison of state-of-art LC VCOs.

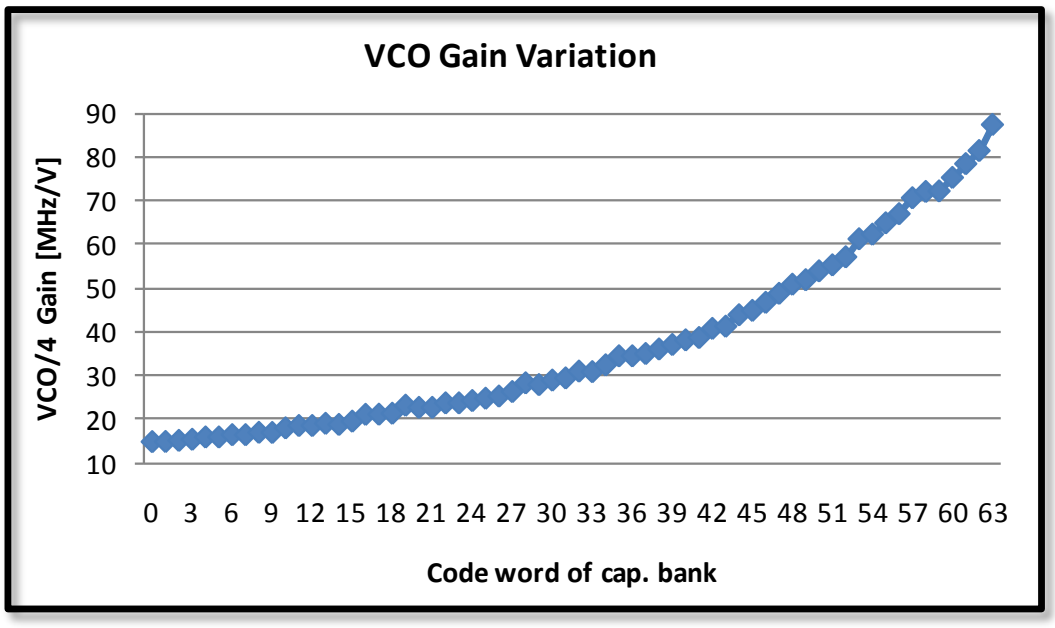


Figure 6.31. Variation of Kvco/4 according to each code word.

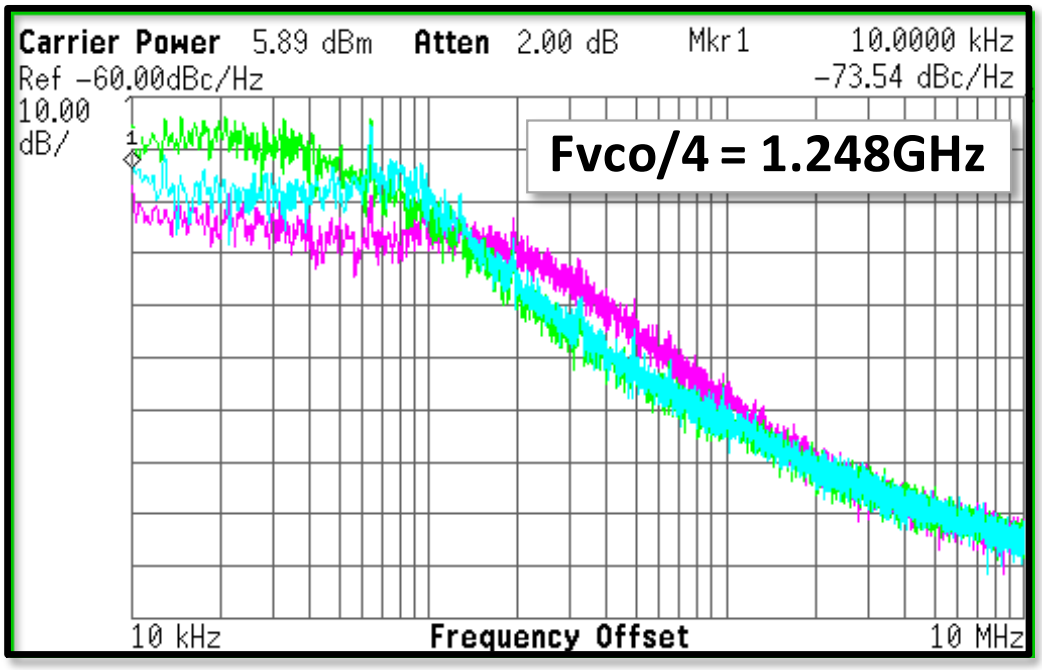
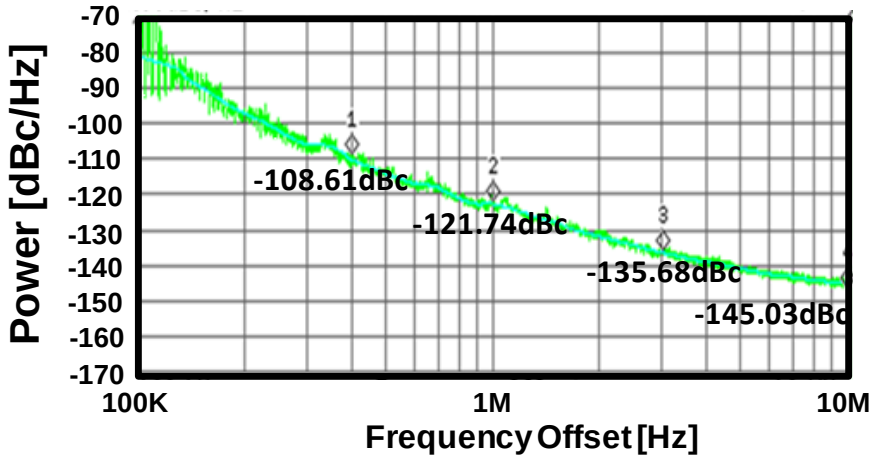
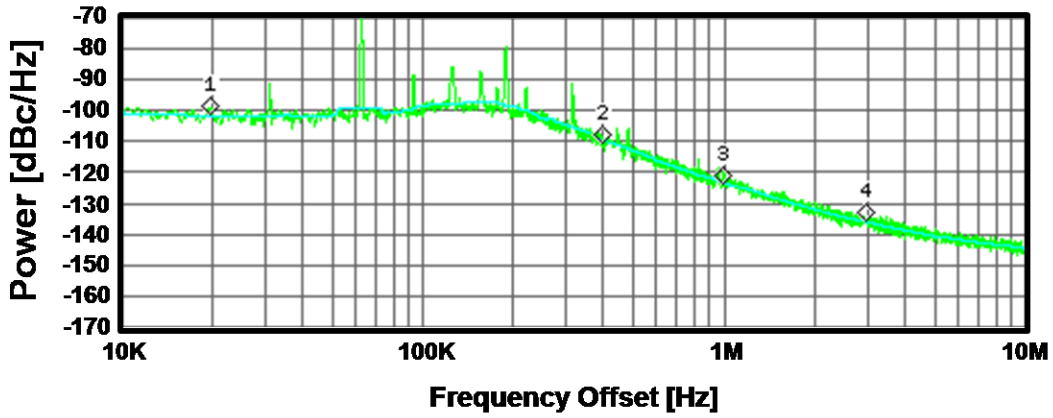


Figure 6.32. PLL bandwidth control with the CP currents (Fosc = 1.248 GHz).



Marker	Frequency offset	Phase noise
1	400 KHz	-108.61 dBc/Hz
2	1 MHz	-121.74 dBc/Hz
3	3 MHz	-135.68 dBc/Hz
4	10 MHz	-145.03 dBc/Hz

Figure 6.33. VCO free-running phase noise.



Marker number	Frequency offset [Hz]	Phase noise [dBc/Hz]
1	20 K	-101.45
2	400 K	-110.81
3	1 M	-123.60
4	3 M	-135.58

Figure 6.34. Measured phase noise of the proposed PLL.

The measured results show the in-band phase noise of -101dBc/Hz. From a 1.248 GHz carrier, the out-band phase noise values are -110.81, 123.6, -135.58 and -145.2 dBc/Hz at the offset frequencies of 400KHz, 1MHz, 3MHz, and 10MHz, respectively. The loop bandwidth is 200 KHz as shown in Figure 6.34. The PLL consumes less than 7mA current from a 1.0V supply. Measured reference level is -78.51dBc. Measured performances are summarized in Table 6.1. Figure 6.35 and Figure 6.36 show the layout and micrograph of the prototype chip fabricated in a 45nm SOI-CMOS process. The PLL can support multiples standards including all cellular band such as GSM, EDGE, WCDMA, LTE, and almost all WLAN and WiMax bands. Measurement results demonstrate the PLL is a good solution for multi-standard mobile communication systems.

Table 6.1. Performance summary of the proposed wideband PLL.

Technology	45 nm SOI CMOS
Reference frequency	26 MHz
VCO oscillation frequency range	4.87 ~ 9.65 GHz (65.8%)
Fout (= Fvco/4)	1.22 ~ 2.41 GHz
In-band phase noise (Fout = 1.248 GHz)	-101.45 dBc/Hz @ 20 KHz
Out-band phase noise (Fout = 1.248 GHz)	-110.81 dBc/Hz @ 400 KHz -123.60 dBc/Hz @ 1 MHz -135.58 dBc/Hz @ 3 MHz -145.20 dBc/Hz @ 10 MHz
Reference spur	-85.76 dBc
Loop bandwidth	200 KHz
VCO gain (Kvco/4)	15 ~ 87 MHz/V
Active area	< 0.192 mm^2
Supply voltage	1.0 V
Current	< 7 mA

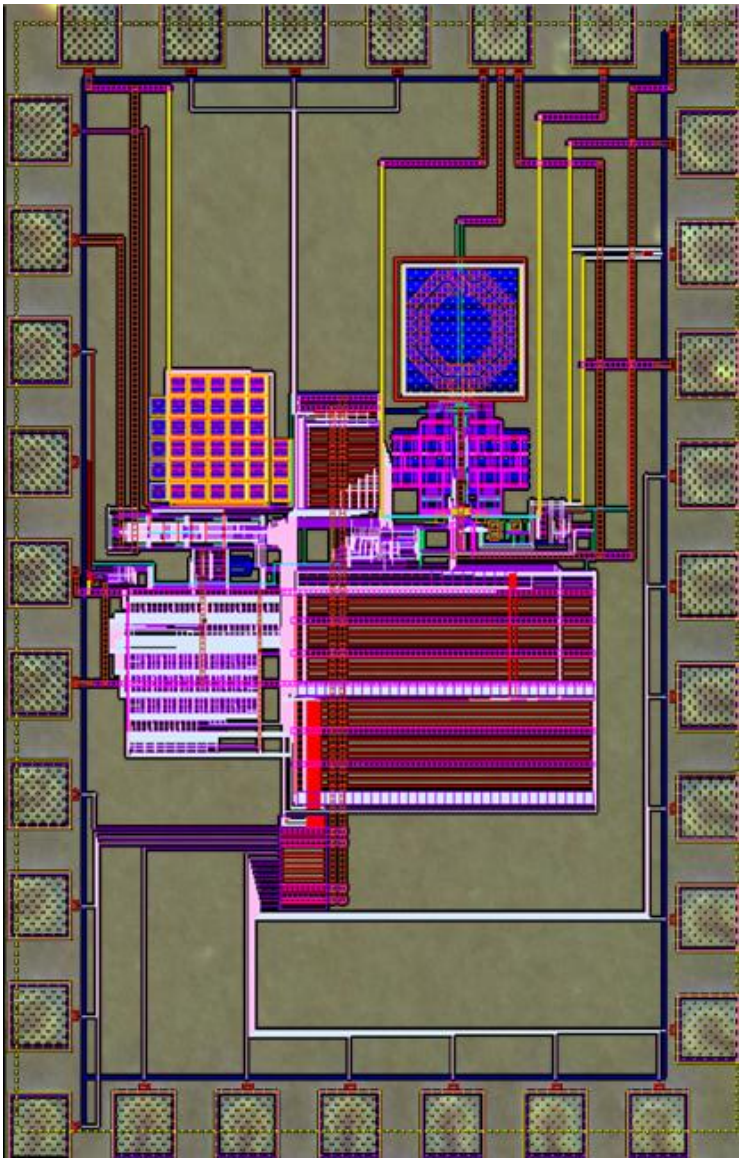


Figure 6.35. Chip layout.

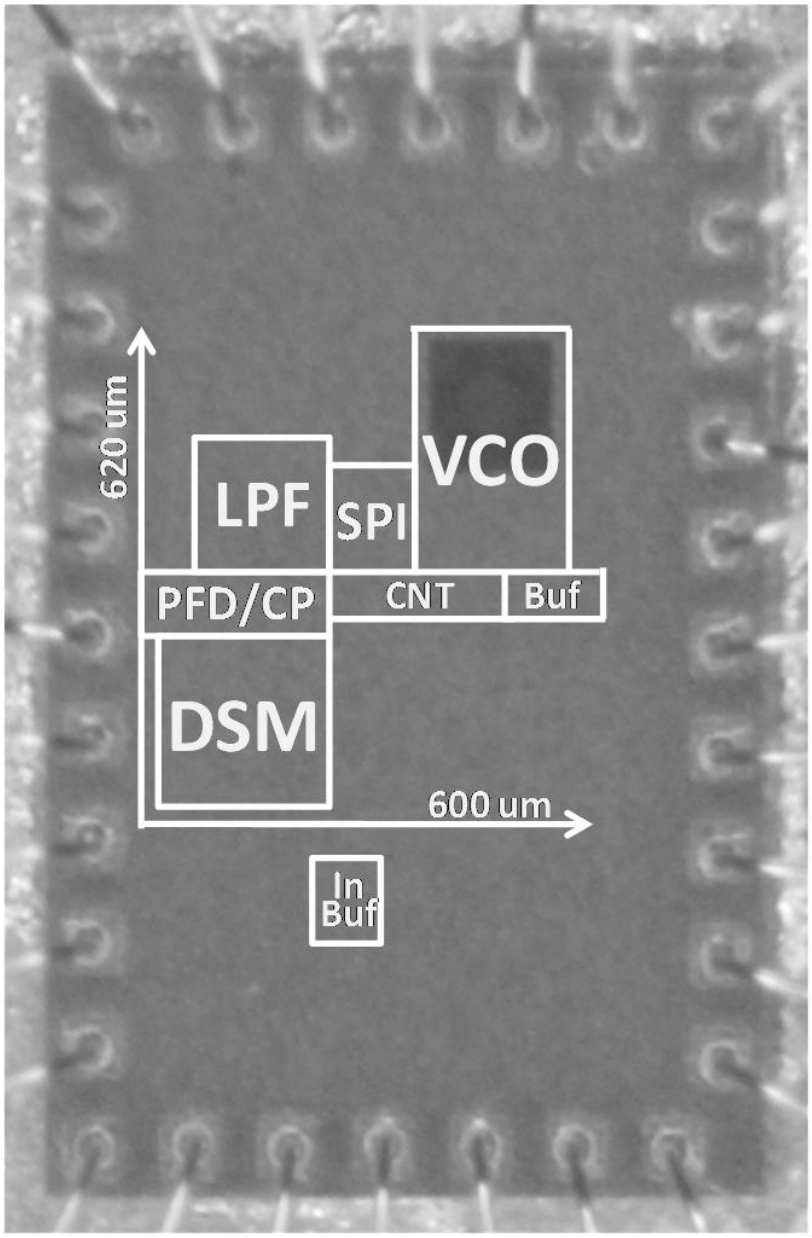


Figure 6.36. Chip photo of the proposed PLL.

It is necessary to design a dedicated control block such as *Serial Peripheral Interface* (SPI) because more than 100 control signals are required for PLL test. Shown in Figure 6.37 is the *Graphical User Interface* (GUI) using Visual Basic to control the PLL via the SPI block.

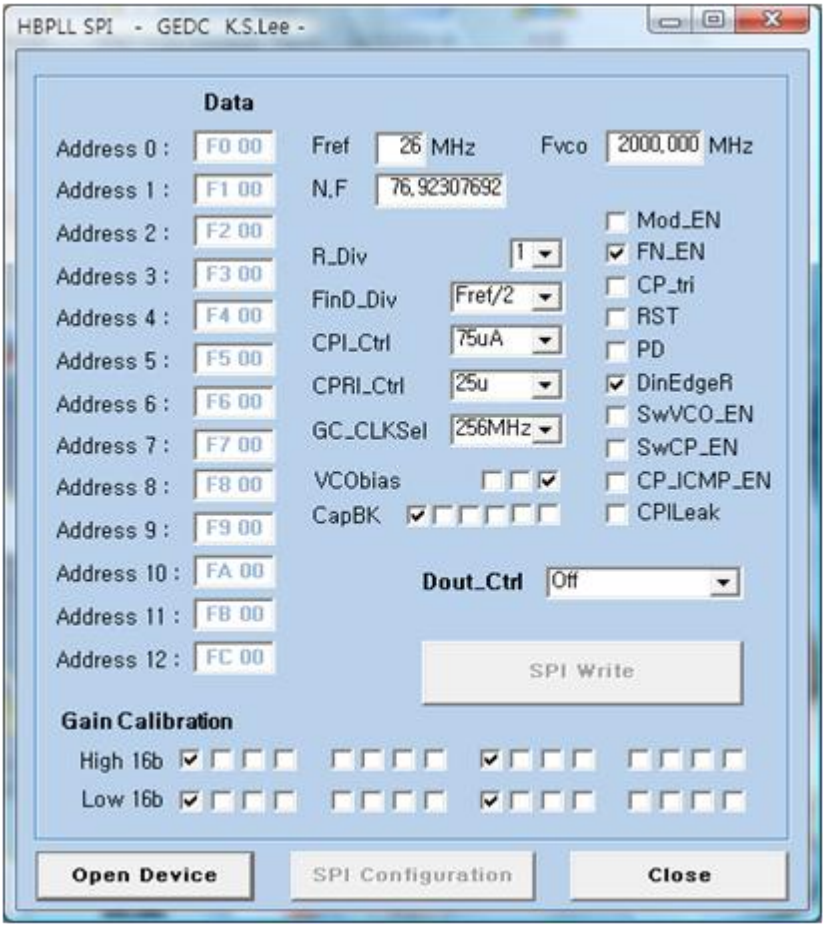


Figure 6.37. GUI using Visual Basic for PLL test.

6.5. Conclusion

In this research, a wideband SOI-CMOS PLL is proposed. The dynamic range reduction of deep sub-micron technologies results in narrow frequency range and phase noise degradation in RF PLLs. To overcome these limitations, the proposed PLL utilizes the advantage of a SOI CMOS technology, small parasitic capacitance and high oscillation frequencies. The capacitance variation range in capacitor bank is maximized to increase the frequency coverage. The capacitor bank using MIM capacitors and simple MOS switches is controlled by a binary 6-bit digital codes and generates 64 VCO transfer curves. The measured frequency range from 4.87GHz to 9.65GHz demonstrates the proposed PLL can be a good solution for a transceiver supporting multiple-standard services. The oscillation frequency of the VCO has been increased to save die area and to increase Q-factor of the inductor in a LC-tank. Since the Q-factor of the inductor dominates the phase noise performance of a LC-VCO, this method compensates the increased phase noise levels due to the dynamic range reduction of deep sub-micron technologies. The measured phase noise also shows good performance. The total chip area is less than $0.192mm^2$.

CHAPTER 7

CONCLUSIONS

To follow the main trends in the mobile communication systems, the high integration with scaling down to deep submicron and multiple-standard supporting services are strongly requested. A RF PLL has an important role in transceivers for mobile communication systems because it generates high frequency RF signals and the RF signals convert baseband data to the modulated high frequency data and vice versa. Thus, the spectral purity of the RF signals is closely related to service quality, and wide frequency coverage is essential to support multiple standards. In this dissertation, a wideband RF CMOS PLLs with high spectral purity using deep sub-micron technologies is implemented.

In order to design RF PLLs for mobile communication systems, this dissertation gives some motivations of this research by over viewing some trends in mobile communication systems and the roles of PLLs in RF transceivers. Additionally, the operation and design considerations of PLLs and basic building blocks are studied before introducing a new wideband RF PLL. The achievements from this dissertation can be summarized as follows

A new third order sample-hold loop filter in a RF CPPLL is proposed. It uses two MOS switches for high spectral purity. One switch is used to improve in-band phase noise of the PLL by giving enough settling time after the PLL loop reconnection. This reduces the fluctuation range of the VCO tuning node. By using another switch, the CP

switching noise and the induced noise from supply and ground planes are not directly coupled to the LPF when the CP is activated. High-frequency noise bypasses through the first coming capacitor of the LPF and the out-of-band phase noise performance is improved. The proposed loop filter provides up to 8 dBc/Hz phase noise improvement in in-band and 9 dBc/Hz in out-of-band.

A wideband SOI-CMOS PLL is proposed. The dynamic range reduction of deep sub-micron technologies results in narrow frequency range and phase noise degradation in RF PLLs. To overcome these limitations, the proposed PLL utilizes the advantage of a SOI CMOS technology, small parasitic capacitance and high oscillation frequencies. The capacitance variation range in capacitor bank is maximized to increase the frequency coverage. The measured frequency range from 4.87GHz to 9.65GHz demonstrates the proposed PLL can be a good solution for a transceiver supporting multiple-standard services.

Each block in the RF PLL is also optimized depending on each critical design issue. To improve the PFD/CP nonlinearity, a static leaking current is inserted, and a delay buffer is used to reduce path delay difference between two signals. In the CP, a programmable control scheme is used to compensate the PLL bandwidth variation due to the VCO gain change. A 4-bit control signal with a 25-uA unit current cell is used. By doing this, the current control range is extended to 400 uA with a monotonic increment. A 3-bit third order DSM is designed and used. System simulation is done with a Simulink model to guarantee the stable operation. A 4/4.5 phase switching type prescaler is designed and it realize 0.5 division ratio so that the quantization noise level from DSM can be reduced.

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VITA

Kun-Seok Lee was born in Busan, Korea, in 1972. He received the B.S and M.S degrees in electronics engineering from Korea University, Seoul, Korea, in 1999 and 2001, respectively. He is currently working toward the Ph.D. degree in electrical and computer engineering at Georgia Institute of Technology. From 2001 to 2008, he was with the Samsung Electronics, where he was a senior engineer involved in the design of sigma–delta FN PLLs and PLL-based transmitters for CDMA/GSM/GPRS/EDGE transceivers. His current research is focused on RF/analog integrated-circuit design supporting multiple standard options for wireless applications and CMOS power amplifiers. He was the recipient of the Best Design Award at the 1st National Semiconductor IC Design and Layout Contest, Korea, in 2000.